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MAY 1974

FINAL TECHNICAL REPORT

FREQUENCY CONVERTER PORTABLE, ALTERNATING CURRENT MULTIFREQUENCY, 10 KW

VOLUME I

Contract CDRL Item A002

Contract No. DAAK 02-72-0210

Submitted to

U.S. ARMY MOBILITY EQUIPMENT
Research and Development Center
Fort Belvoir, Virginia

Delco Electronics

General Motors Corporation
- Santa Barbara Operations
Santa Barbara, California

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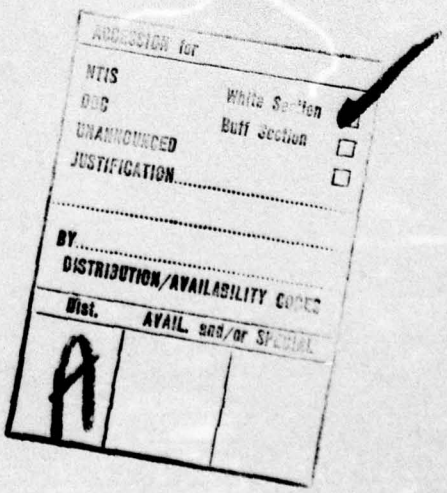


SECTION I
INTRODUCTION

1.1 BACKGROUND

The Delco Electronics three-phase static frequency converter uses the Power Center approach to precision waveform generation. With this technique, 80% of the power to the load is controlled directly by a thyristor bridge circuit between a dc voltage supply and a three-phase load. The remaining 20% of the power is transferred to the load via a series of low impedance taps on an autotransformer. The taps are sequentially connected to the load such that a low harmonic content, stair-step approximation to a sine wave is provided. The purpose of this project was to determine the applicability of the Delco inverter design approach to the development of Army portable frequency converters. Statement of Work requirements of the project are shown in Table 1-1.

1.2 OBJECTIVES

The initial phase of the project (Item 0001) was the development of a breadboard circuit capable of performing all the electrical functions of a three phase frequency converter, as defined in Attachment No. 1 of the contract. After demonstration of three phase performance, the work scope was extended (Item 0003) to further develop the breadboard circuits to produce 10 kW of single phase power at 60 Hz or 400 Hz.

Concurrent with development of the 10 kW frequency converter, Delco developed improved step voltage commutation methods for a 100 kW frequency converter under MERDC Contract No. DAAK 02-72-C-0338. Since some circuit advances were applicable to the 10 kW frequency converter, the work scope was enlarged (Item 0004) to incorporate the new circuits into the breadboard.

After three phase and single phase performance was demonstrated, an additional investigation (Item 0005) was added to the work statement. This involved demonstration of 15 kVA three-phase and 10 kVA single-phase operation of the breadboard, study of voltage regulation methods for operating the frequency converter from utility power, and performance of regulation tests with a Delco developed voltage regulation system.

ITEM NO.	SUPPLIES / SERVICES
	E.1. The Contractor shall furnish all engineering, labor, tools, services, supplies, materials, equipment and facilities necessary and design, assemble, test and deliver a prototype (breadboard) Frequency Converter Unit, Portable Alternating Current, Multifrequency, 10 kW, in accordance with the electrical performance criteria of Attachment No. 1, listed in Section F (below) except that the motor starting performance specified in Paragraph 3.24.4 therein shall not be provided. E.2. In connection with, and as a part of, the above work and services the Contractor shall furnish the following items:
0001	One (1) each prototype (breadboard) converter designed and tested to meet all of the electrical performance criteria specified in Attachment No. 1 for the engineer design test (EDT) model, with all components designed to meet the size and weight constraints, but not packaged for the full range of environmental and transportation requirements.
0002	Data, in accordance with DD Form 1423, Contract Data Requirements List, marked Exhibit "A".
0003	The Contractor shall furnish all engineering, labor, tools, services, supplies, materials, equipment and facilities necessary to modify the frequency converter unit furnished as Item No. 0001, to comply with the electrical performance criteria of Attachment No. 3, except that the motor starting performance specified in Paragraph 3.24.4 therein shall not be provided. This attachment is an updating of Attachment No. 1 in that it contains some editorial and typographical corrections and also requires that the output of the frequency converter unit be reconnectable for either single phase or three phase output voltages. This effort shall be accomplished through the following tasks: • Task 1: The Contractor shall conduct an engineering investigation to define the most appropriate design approach to meet the single and three phase output requirements of Attachment No. 3. This effort shall consider, but not be limited to, such parameters as effects on production costs, overall weight and technical objectives. The Contractor shall schedule an informal technical review at the end of this effort for presentation of findings to the Contracting Officer's Representative. • Task 2: The Contractor shall furnish the necessary engineering, labor, tools, services, materials, equipment and facilities to fabricate the circuit design selected in Task 1, install the circuit in the frequency converter unit and perform sufficient testing to demonstrate conformance with electrical performance requirements of Attachment No. 3 when powered from a laboratory dc power source. • Task 3: At the conclusion of Task 2, the Contractor shall analyze and modify the frequency converter unit, as necessary, to enable it to perform in conformance with the electrical performance requirements in Attachment No. 3 when operating with power input from the high speed Turbo-Alternator furnished as GPF under Paragraph J.4.3., "Special Provisions."
0004	The Contractor shall furnish all engineering, labor, tools, services, supplies, materials, equipment and facilities necessary to upgrade the commutation capability of the frequency converter (furnished as Item 0001) to enhance to the maximum extent possible the operation of the frequency converter when energizing single phase, 0.5 per unit impedance, low power factor loads. This effort shall include, but not necessarily be limited to, the step voltage commutation methods developed in Contract DAAK 02-72-C-0338.
0005	The Contractor shall furnish all engineering, labor, tools, services, supplies, equipment and facilities to adapt the frequency converter (furnished as Item 0001) to operation from 120/208 volts, 3 phase, 50 or 60 Hz power sources. The frequency converter shall then function as a power conditioner in accordance with the electrical output performance requirements of Attachment No. 3 listed in Section F, except that at three phase, the rated output shall be 15 kVA. This output performance shall apply for an input frequency variation of plus or minus 10 Hz, and a voltage variation from plus 10 percent to minus 15 percent. These voltage and frequency variations shall occur in any combination. The attenuation of power perturbations at the input shall be maximized and the input impedance presented to the line shall be essentially linear. This effort shall be accomplished through the following tasks: • Task 1: Perform an investigation and analysis of practical circuit schemes that can be used to regulate the frequency converter output voltage, attenuate source inducted voltage disturbances, linearize input impedance, and provide current limiting. • Task 2: Develop design data test procedures for the voltage regulator, current limiter system. • Task 3: Perform design data testing. • Task 4: Analyze test data for inclusion in final report.

Table 1-1. Contract Statement of Work Requirements

1.3 SUMMARY OF RESULTS

In performance tests, the three-phase breadboard developed under Item 0001 demonstrated the capability of meeting nearly all the requirements of Attachment No. 1 of the contract. The test results are documented in Volume II of this report. Significant deviations from requirements were:

- Deviation factor for 60 Hz operation greater than 5 percent,
- The 41st harmonic slightly exceeded 2% at 60 Hz,
- Voltage unbalances slightly greater than 5 percent were measured for the unbalanced load tests at 400 Hz and 60 Hz.

During the investigation under Item 0003 it was determined that the most efficient method of obtaining single phase power from the breadboard was by means of a single phase auto-transformer connected from line-to-line. Voltage taps were designed to produce two-wire or three-wire power. The significant negative effect was an increase in inverter weight of 40 lb.

Breadboard performance tests were made after the completion of Item 0004, upgrading of commutation capability. Tests results, documented in Volume II, show that the frequency converter meets most of the performance requirements of Attachment No. 3 of the contract. Significant deviations from the requirements were:

- Deviation factor for 60 Hz operation greater than 5 percent,
- Maximum power output of only 8.5 kW at 60 Hz single phase 0.8 PF,
- Excessive third harmonic for single phase operation.

Tests completed under Item 0005 show that the frequency converter can produce 15kVA three-phase or 10kVA single-phase power at 60 Hz or 400 Hz. By combining the frequency converter with a Delco regulator to form an experimental power conditioner, it was demonstrated that the voltage regulation and transient requirements of Attachment 3 could be met for three phase operation. Further development is required for current limiting, current harmonic reduction in the input lines, and voltage regulation for single phase operation.

In summary, the problem areas in terms of electrical performance have been studied and only a moderate development effort is required to make the breadboard frequency converter capable of meeting all the requirements of Attachment No. 3. Test results are included in Volume II. Conclusions are summarized in Section II of this report.

SECTION II
PROJECT DETAILS

2.1 DESIGN AND TEST OF PROTOTYPE CONVERTER (ITEM No. 0001)

Item No. 0001 was the design of a breadboard 10 kW frequency converter as illustrated in Figure 2-1. The frequency converter can be operated from the output of the turbo-alternator which produces 1,550 Hz three-phase power at voltages approximately 120/208 V rms, or from dc voltages (nominally ± 140 Vdc). Output voltages and frequencies produced are:

- Three-phase, four-wire, 60 Hz, 120 volts line-to-neutral and 208 volts line-to-line (120/208 volts) at 10 kW, 0.8 power factor.
- Three phase, four-wire, 400 Hz, 120/280 volts at 10 kW, 0.8 PF.

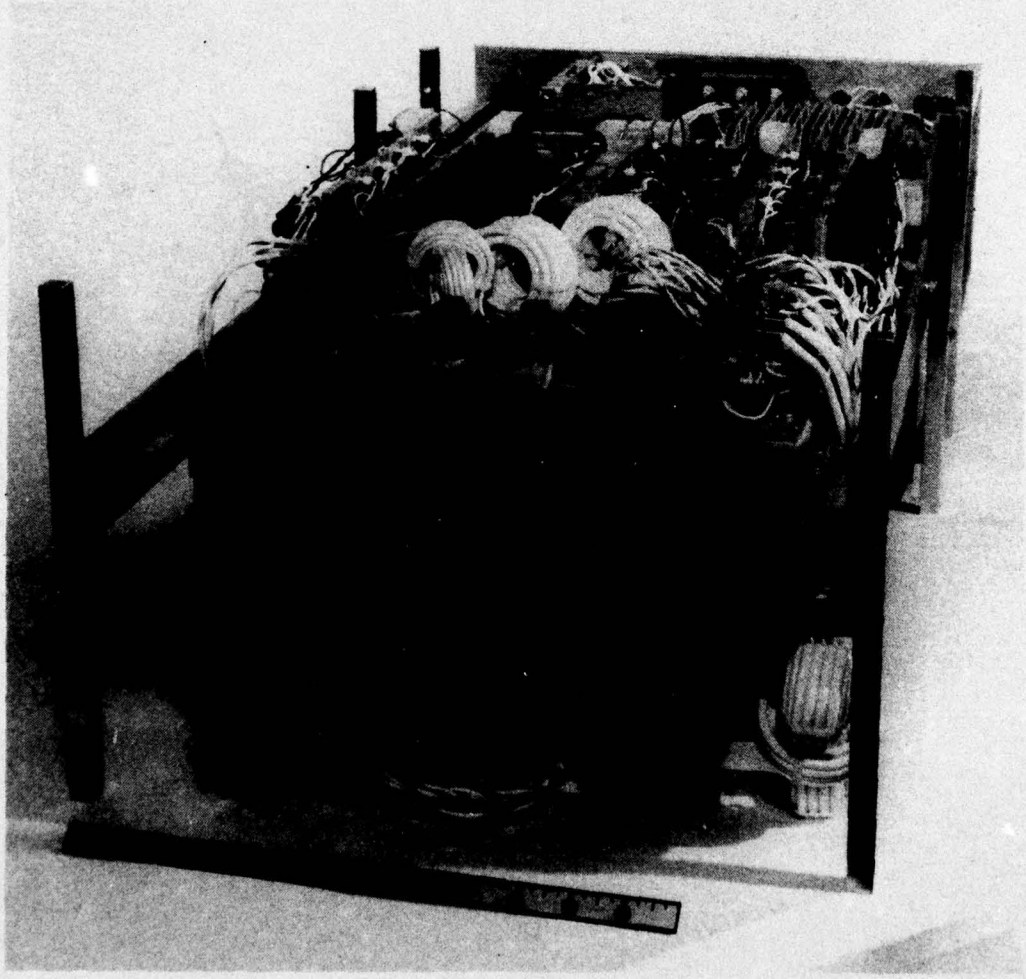


Figure 2-1. Item 0001. Breadboard 10 kW Frequency Converter

The 10 kW frequency converter breadboard was required to operate in accordance with the electrical performance criteria of Attachment No. 1 of the contract. Documentation of the Item No. 0001 breadboard performance tests, conducted in accordance with MIL-STD-705B, is located in Volume II of this report.

2.1.1 INSTALLATION AND OPERATION

The schematic diagram in Figure 2-2 shows how the Item No. 0001 10 kW frequency converter is connected to the turbo-alternator power source and the load bank. Additional ac power is required to operate the cooling fans and 28 Vdc is needed to energize the frequency converter auxiliary power supplies. The connections shown are all that are needed to get the system operating. Before a load is applied, the output frequency select switch (60 or 400 Hz) should be in the desired position.

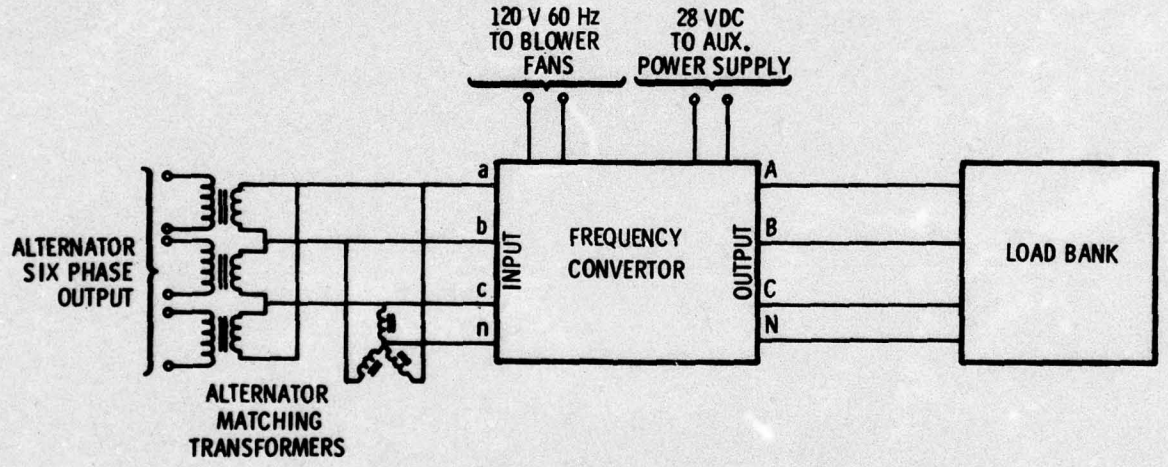


Figure 2-2. Schematic Diagram Showing Installation of Item No. 0001, 10 kW Frequency Converter

Frequency converter output voltage is controlled by the alternator field control circuit. Once connected, as shown in Figure 2-2, Item No. 0001 requires no further attention other than the operation of the output frequency select switch.

2.1.2 DESCRIPTION OF CONVERTER SUBSYSTEMS

Figure 2-3 is a block diagram of the complete frequency converter. The power handling portions of the system are the rectifier-input filter, inverter, and output filter. The

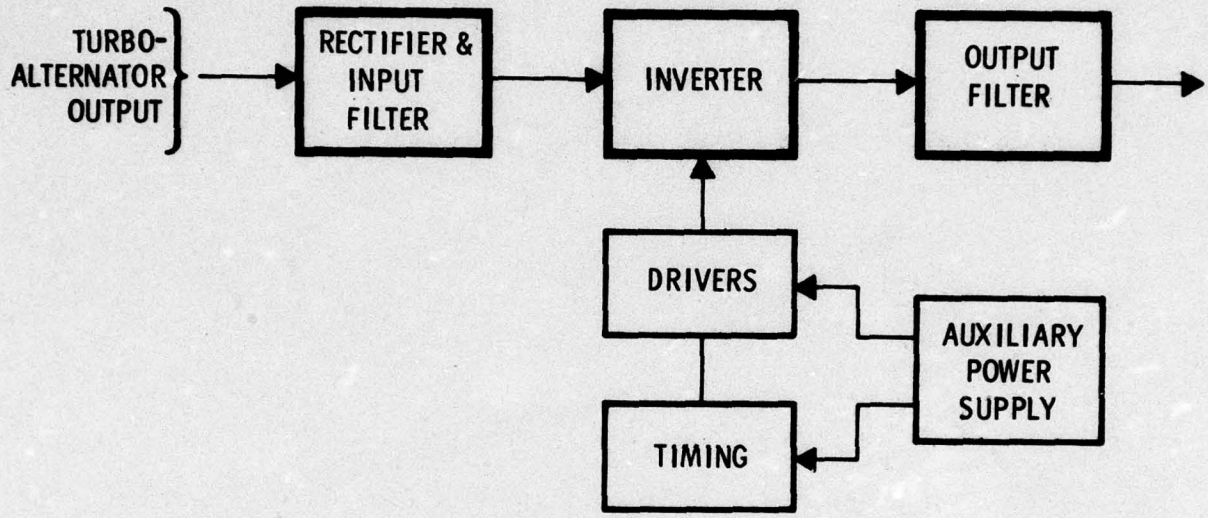


Figure 2-3. Basic Frequency Converter Elements

inverter is controlled by the timing and driver circuits. A small auxiliary power supply is required to energize the timing and driver circuits.

2.1.2.1 Inverter

A detailed description of the development of the Delco Inverter concept is provided in Appendixes B and C of Volume II. As shown in Figure 2-4, the Delco inverter consists of three power switch circuits that generate squarewave and stepped voltages which are combined on the three phase output line to produce low harmonic approximations to sine-wave voltages. The power switch circuits generate three voltages which are designated the center, y and x functions, and are defined by the waveforms of Figures 2-4 and 2-5. The y and x voltage steps are produced by using a tapped autotransformer energized by a square wave voltage that is three times the inverter output frequency. Two sets of thyristors are connected to the transformer taps; one set produces the y voltage steps, and the other the x voltage steps. The center voltages are produced by a square wave switching circuit which operates in synchronism with the y and x voltages, but is 180° out of phase.

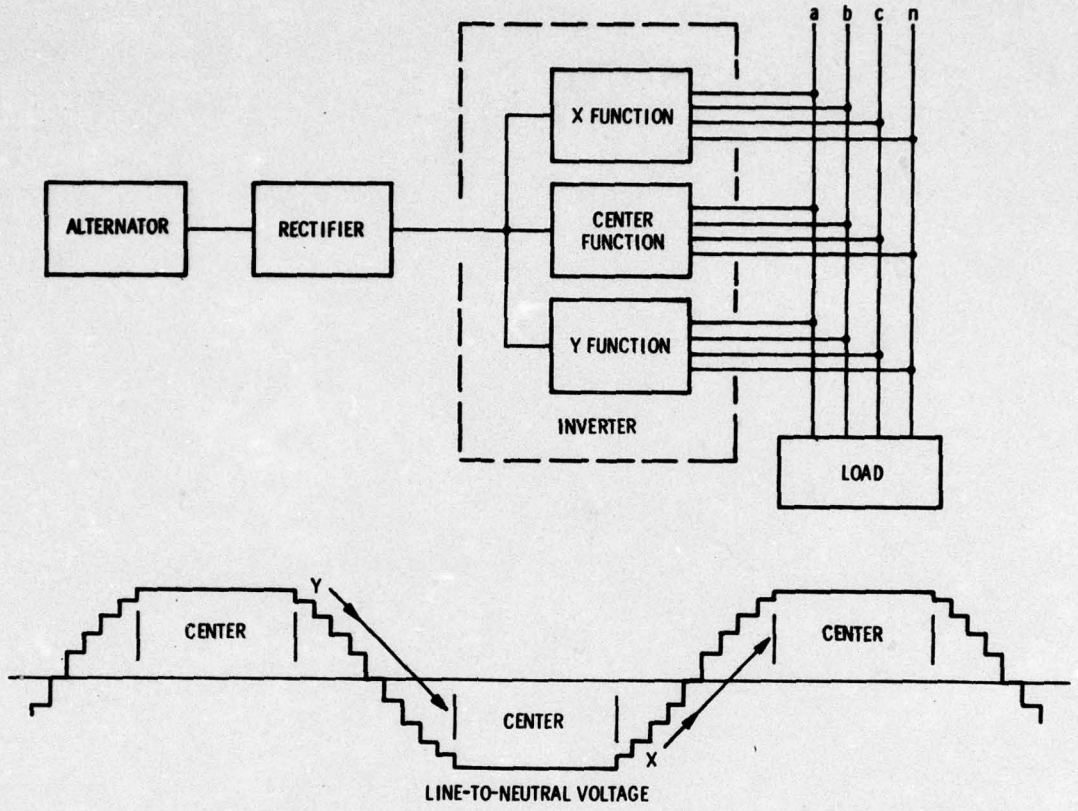


Figure 2-4. Power System Block Diagram and Stepped Waveform

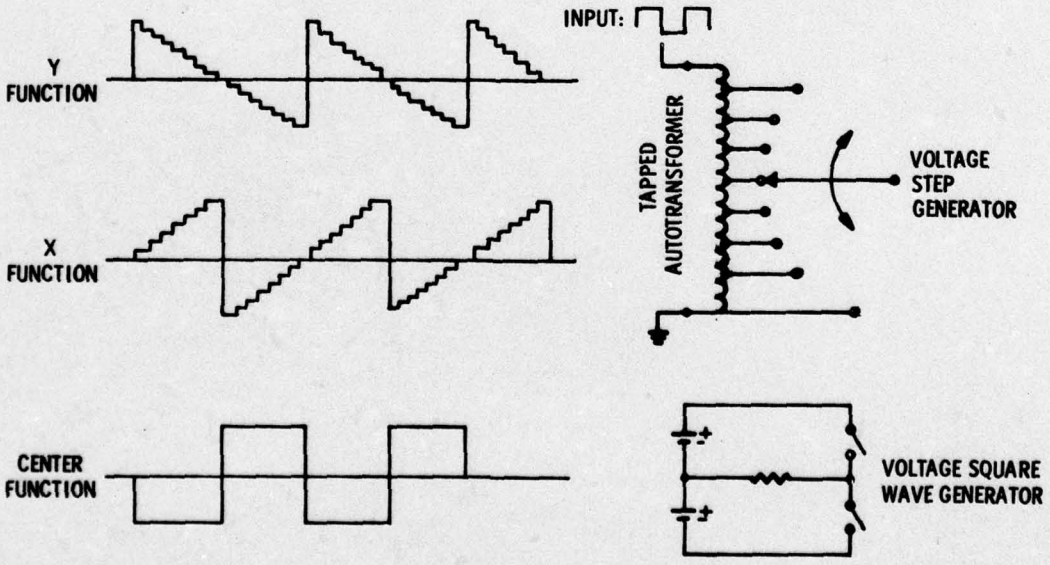


Figure 2-5. Definition of y, x and Center Functions and Originating Circuitry

The waveform designed for the inverter is illustrated in Figure 2-6. This waveform has a flat top portion that is 99° wide and allows the "center" switches to deliver more than 80 percent of the power when inverter voltages and currents are in phase. The steps are 9° wide. Total harmonic content of the line-to-line wave is 4.2 percent. Table 2-1 lists the individual harmonics of the line-to-neutral voltages up to the 63rd harmonic.

L-N Voltage Harmonic	Voltage as % of Fundamental	L-N Voltage Waveshape	
		Degrees	Voltage
1	100.0	0.0	0.00
3	16.02	4.5	0.28
5	0.19	13.5	0.52
7	0.61	22.5	0.71
9	1.06	31.5	0.86
11	0.65	40.5	1.00
13	0.51	134.5	1.00
15	0.40	139.5	0.86
17	0.36	148.5	0.71
19	0.33	157.5	0.52
21	0.27	166.5	0.28
23	0.30	175.5	0.00
25	0.22		
27	0.27		
29	0.22		
31	0.34		
33	0.11		
35	0.01		
37	1.28		
39	2.59		
41	2.45		
43	1.10		
45	0.02		
47	0.07		
49	0.21		
51	0.12		
53	0.13		
55	0.09		
57	0.12		
59	0.09		
61	0.10		
63	0.09		

- Power Center Width: 99°
  Step Width: 9°
- No. L-N Voltage Levels: 6
- L-N Total Harmonic Distortion: 16.9%
- L-L Total Harmonic Distortion: 4.2%

Table 2-1. Zero Dwell MERDC 10 kW Inverter Waveform

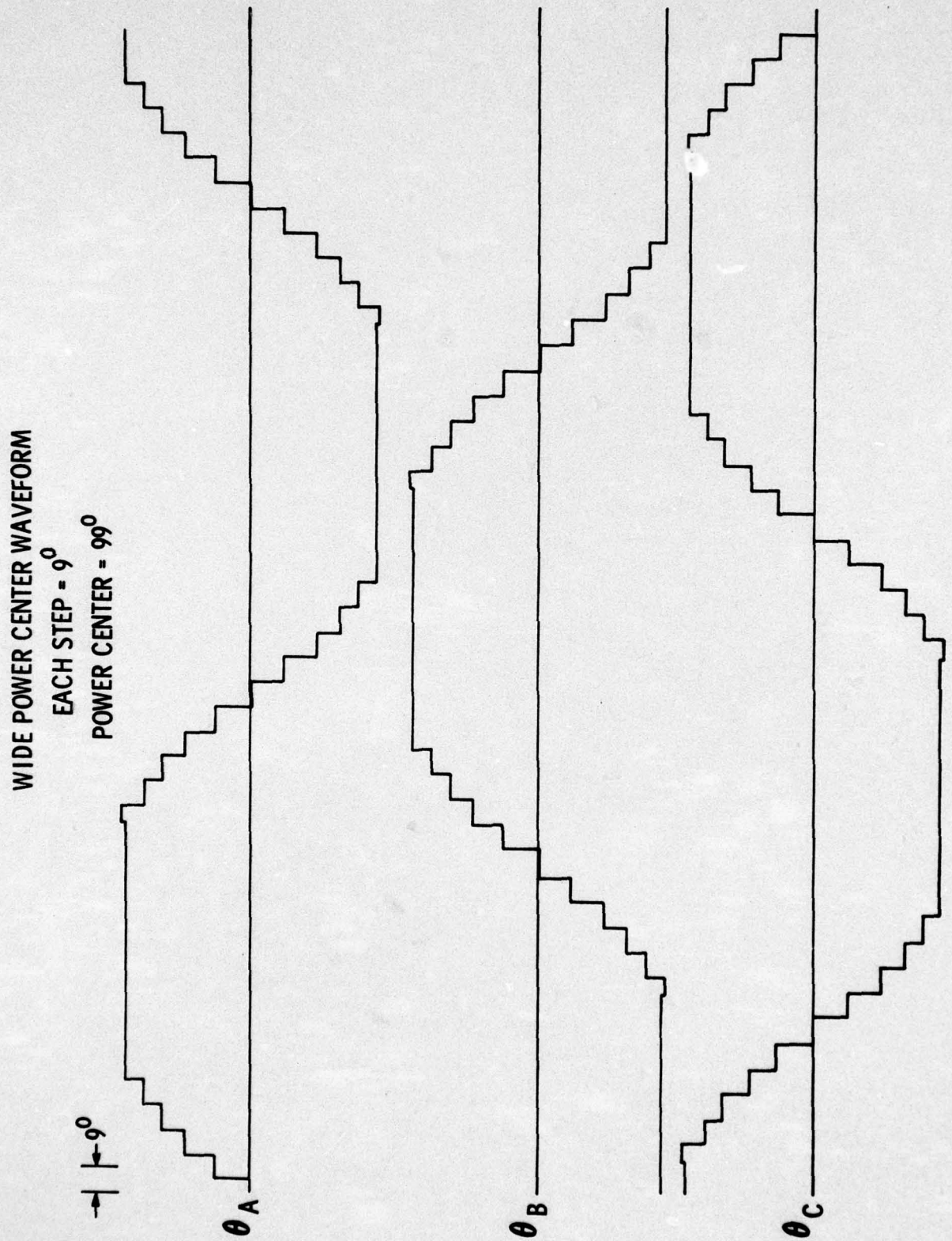


Figure 2-6. Inverter Voltage Waveform Format Used with the MERDC 10 kW Frequency Converter

Note that the magnitude of the third harmonic is 16.02 percent in the line-to-neutral voltage of the inverter. The third and all multiples of the third harmonic (triplens) are reduced to nearly zero by a triplen attenuator at the output of the inverter. Because of the nature of three phase systems, triplen frequencies do not appear in the line-to-line output voltages. Figure 2-7 is a graphical representation of the non-triplen harmonics in the basic inverter voltages up to the 43rd harmonic.

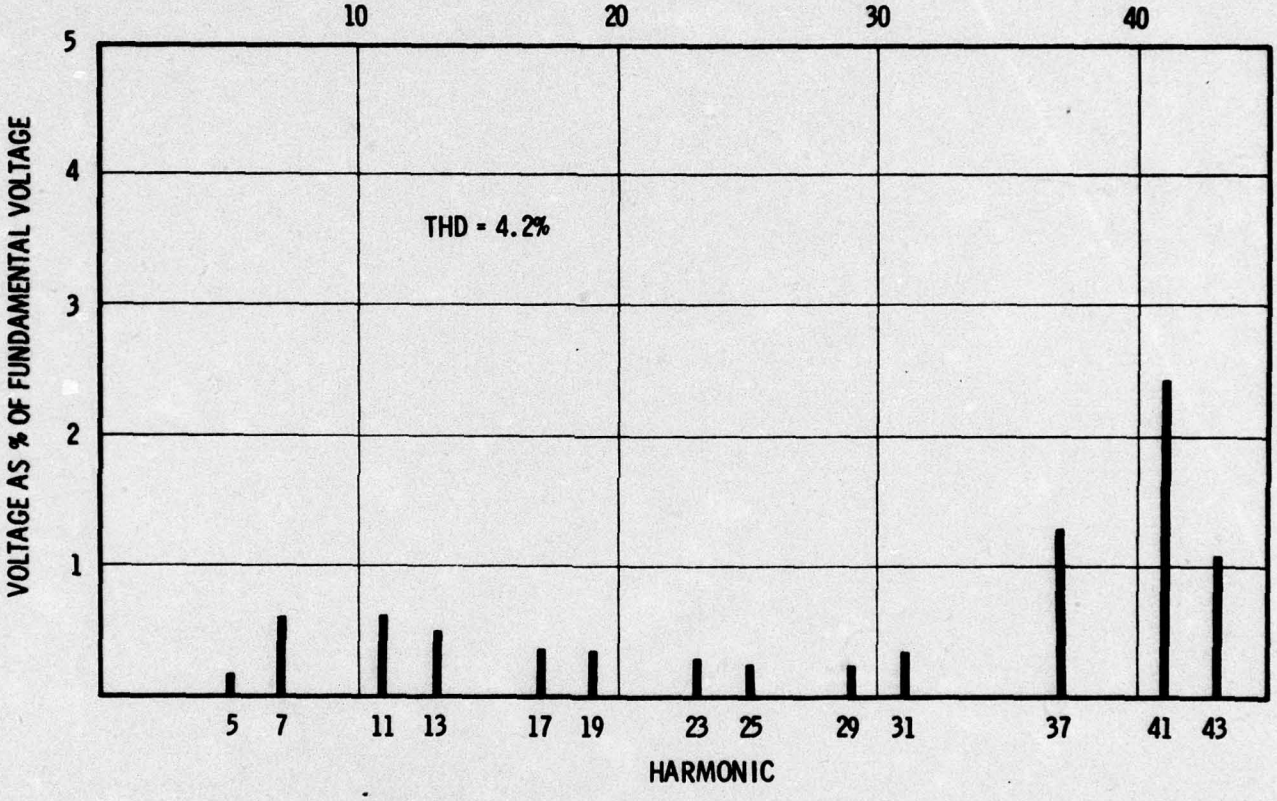


Figure 2-7. Illustration of all Non-Triplen Harmonics in the Basic Inverter Voltage Waveforms up to the 43rd Harmonic

Figure 2-8 is a schematic of Item 0001 10 kW frequency converter, showing the inverter, rectifier, and input and output filters. The inverter consists of:

- A three-phase thyristor bridge circuit that generates the "center" voltage functions,
- Autotransformer-switching circuits that generate the y and x step voltages.

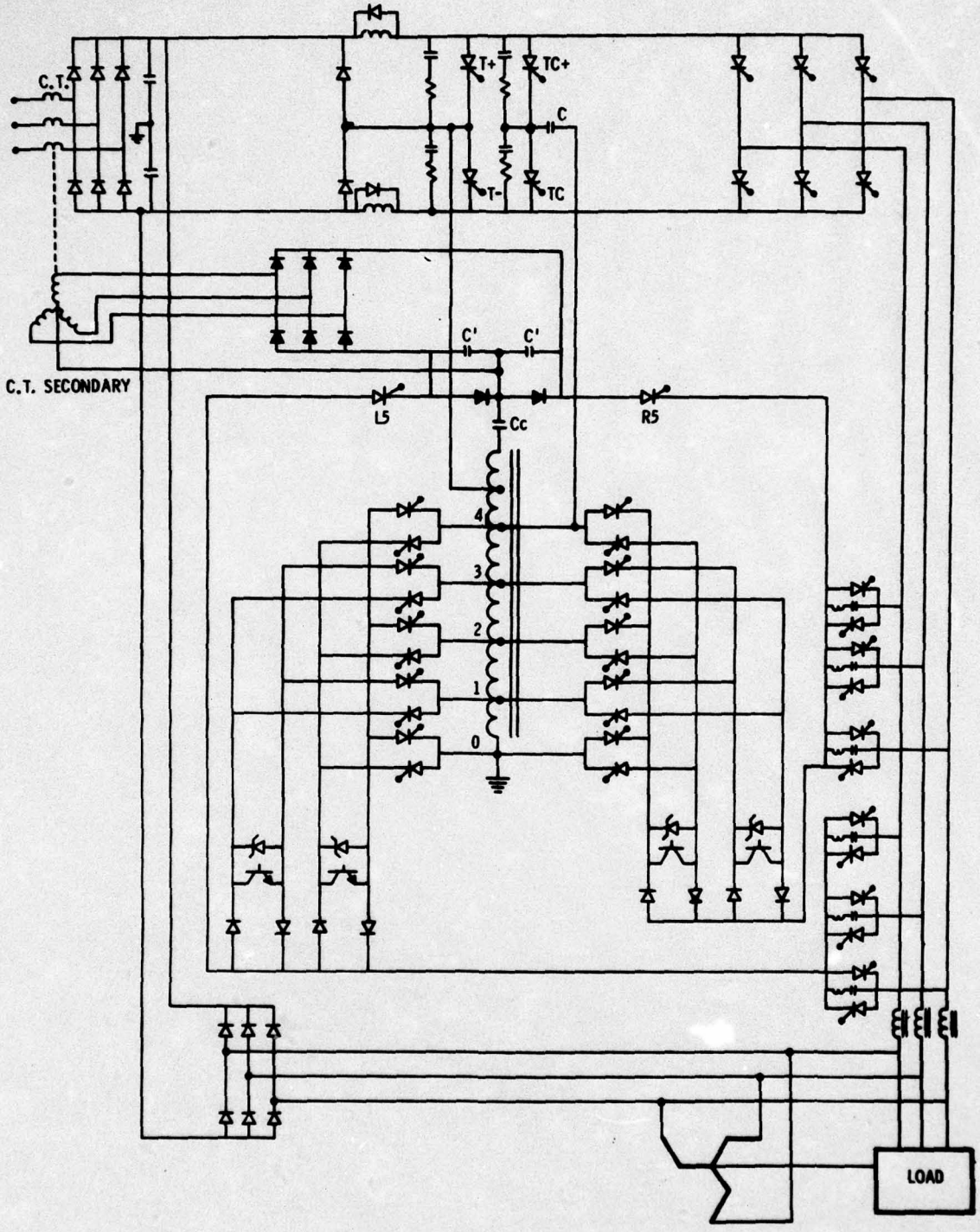


Figure 2-8. Power Circuit Schematic of 10 kW Frequency Converter

- Two sets of phase selector thyristors that sequentially connect the step function voltages to the proper three phase lines,
- A set of reactive return diodes that return energy stored in the load to the dc voltage source,
- A triplen attenuator,
- A zig-zag transformer.

Most of the inverter power passes directly from the power source through the rectifier and center switches and into the output filter and load. This is a very low impedance, high efficiency path. The major losses are the conduction losses of the rectifier and "center" thyristors. The remaining power is carried by the step autotransformer circuit. The step voltage power passes from the power source through a thyristor squarewave switching circuit that energizes the autotransformer, through the appropriate y and x step voltage levels, and to the proper output line by means of the phase selectors. The impedance of this circuit consists of several semiconductors in series with the transformer leakage inductance.

2.1.2.1.1 Thyristor Commutation

The currents of the step selector thyristors pass through transistors that turn off the thyristors by means of current starvation. A thyristor requires a minimum anode current to maintain it in a conducting state. If the anode current drops below this minimum level (called holding current), the thyristor reverts to the forward blocking or off state.

The basic starvation commutation circuit is shown in Figure 2-9. Assume that current is flowing from voltage step level through transistor B. Commutation consists of transferring load current flow from voltage step level 1 to level zero by simultaneously switching transistor B off and transistor A on. Turning off transistor B causes the thyristor anode current to drop below the holding current level and turns it off. Because the turn off time of transistor B is greater than the turn on time of transistor A, there is no instant of time in which the load current path is broken. Inverter inductance, or load inductance, then ensures that current flow will transfer from voltage level 1 to level 0 without much change in amplitude during the commutation interval which is 1-2 microseconds. Transistor B then holds the level 1 thyristor in the nonconducting state long enough for it to regain the capability to block forward voltage, typically 10-20 microseconds. When it is switching,

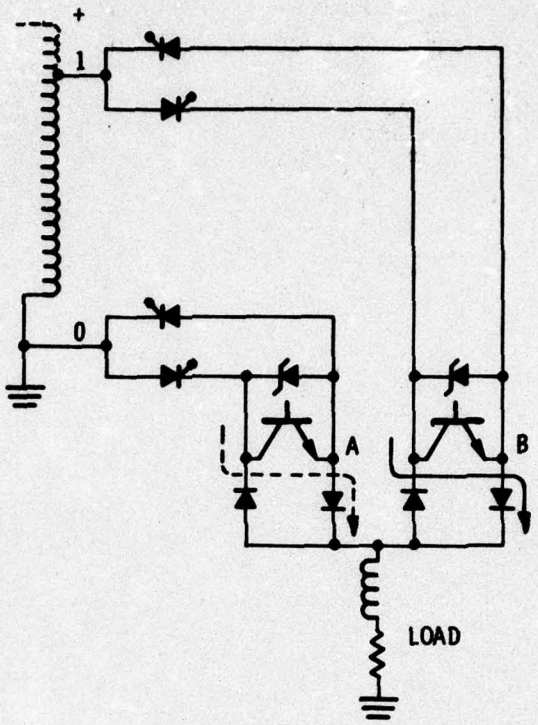


Figure 2-9. Starvation Commutation Step Changing Circuit

transistor B sees a voltage magnitude equal to a step voltage, plus a transient voltage caused by leakage inductance in the step transformer. A typical step voltage might be 30-40 volts. The transient voltage is limited by the zener diode placed across the transistor and does not allow the collector-emitter voltage to exceed 80-90 volts.

Since transistor A is switched on as transistor B is switched off, and sweep-out of excess carriers in transistor B is not instantaneous, there is an interval of time during which voltage step levels 0 and 1 are shorted out. This time interval is typically 0.5 to 1.5 microseconds, insufficient to allow significant rise in short circuit current.

The "center" thyristors of Figure 2-8 are turned off by the reverse voltage commutation circuit, consisting of the top winding of the step transformer, capacitor C_c and thyristors L_5 and R_5. Triggering thyristor R_5 causes commutation current to flow through the appropriate phase selector to turn off the conducting "center" thyristor. Thyristor R_5 turns off "center" thyristors connected to the positive dc voltage line. Thyristor L_5 turns off "center" thyristors connected to the negative dc voltage line.

Thyristors T^+ and T^- of Figure 2-8 are turned off by the commutation circuit made up of thyristors T_c^+, T_c^- and capacitor C. At the time thyristors T^+ and T^- are turned off, only the magnetizing current of the step transformer must be commutated since all load current has been transferred to the "center" thyristors. The magnetizing current is nominally one to two amperes.

2.1.2.1.2 Inverter Waveforms

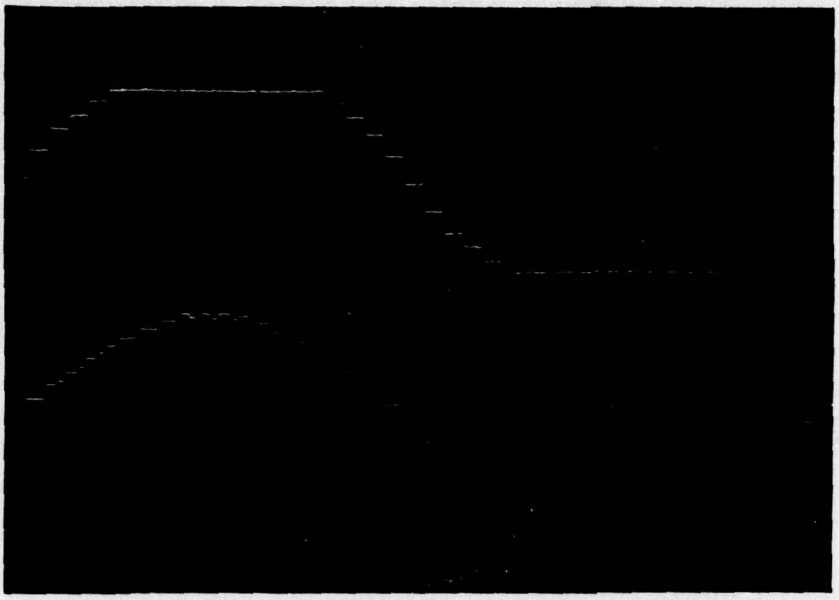
It was mentioned previously that the basic inverter line-to-neutral voltage contains 16.02% third harmonic and that the triplen attenuator reduces all triplen frequencies to near zero. This effect is illustrated in Figure 2-10a, which is an oscilloscope trace of the input and output voltages of the triplen attenuator. The attenuator, which is a relatively high impedance to the triplen frequencies—in combination with the zig-zag transformer, which offers a very low impedance to the triplens—reduces the magnitude of the third harmonic from 16.02% to 0.3% or lower.

The formation of a line-to-line voltage is illustrated in Figure 2-10b. The first two traces are line-to-neutral voltages V_{an} and V_{bn}. The bottom trace is line-to-line voltage V_{ab}. In a three phase system, all triplen frequencies in the line-to-neutral voltages cancel in the resultant line-to-line voltages.

Oscilloscope photographs of the inverter three phase voltages are illustrated in Figures 2-11 through 2-13. The basic inverter flat top, three-phase, line-to-neutral voltages are shown in Figure 2-11. The unfiltered, line-to-neutral voltages at output of triplen attenuator are shown in Figure 2-12. Figure 2-13 shows the unfiltered line-to-line voltages. One cycle of a line-to-line voltage is shown in Figure 2-14.

2.1.2.1.3 Thyristor Package Design and Inverter Assembly

The inverter thyristor packages are specially designed for this inverter to reduce assembly cost and weight. Epoxy encapsulated thyristors (two per package) were used rather than conventional stud mounted types, as illustrated in Figure 2-15. Two, passivated, 110-ampere rms thyristor chips are attached to beryllium oxide insulators soldered to a copper base. The assembly is coated with epoxy resin, with power and gate leads brought out the top. The package is mounted directly on an uninsulated heat sink. Thyristors chips used were International Rectifier 71RCG50 or National Electronics NL-F156E.

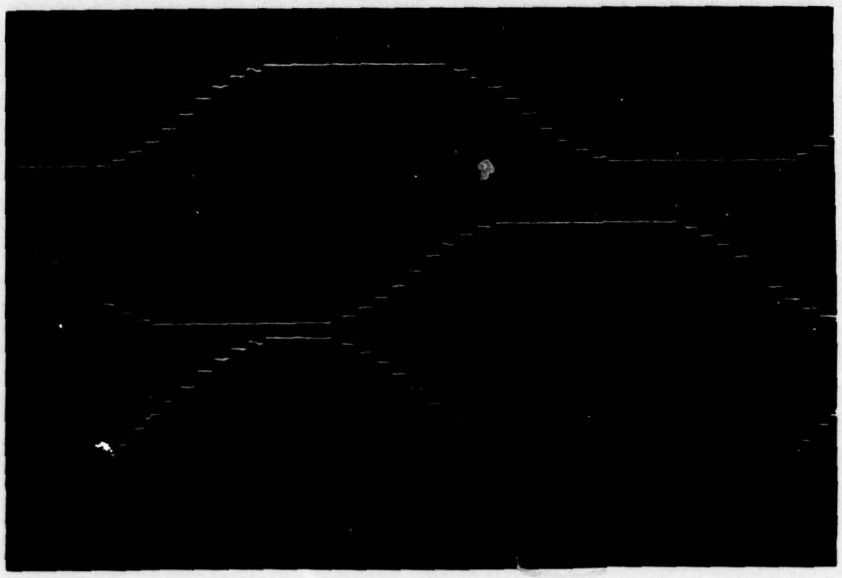


60 Hz, Three-Phase:

Upper Trace: Basic Inverter L-T-N Voltage Into Triplen attenuator.

Lower Trace: Resultant L-T-N Voltage Waveform at Output of Triplen Attenuator. Unfiltered THD = 4.2%

(a)



Upper Traces: Basic Inverter L-T-N Voltages

V_{AN}

V_{BN}

Lower Trace: Resultant Line-to-Line Voltage V_{AB}

$V_{AB} = V_{AN} + V_{NB}$

(b)

Figure 2-10. Input/Output Voltages of Triplen Attenuator

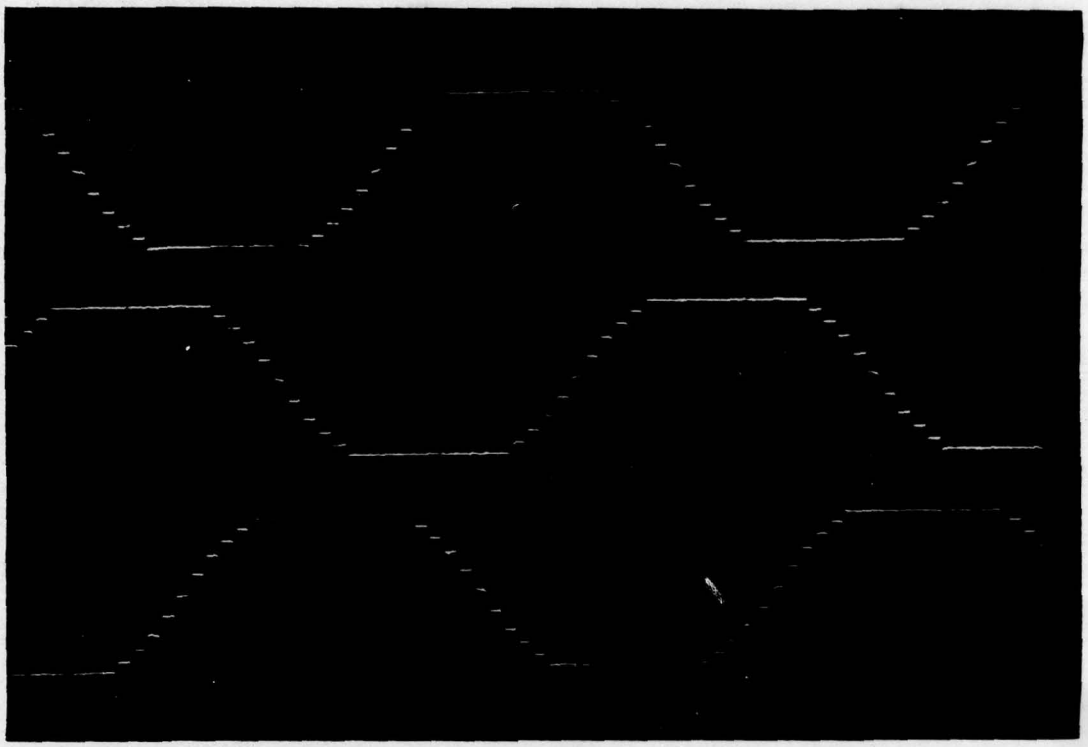


Figure 2-11. Basic Inverter Three-Phase Line-to-Neutral Voltages, THD=16.9%

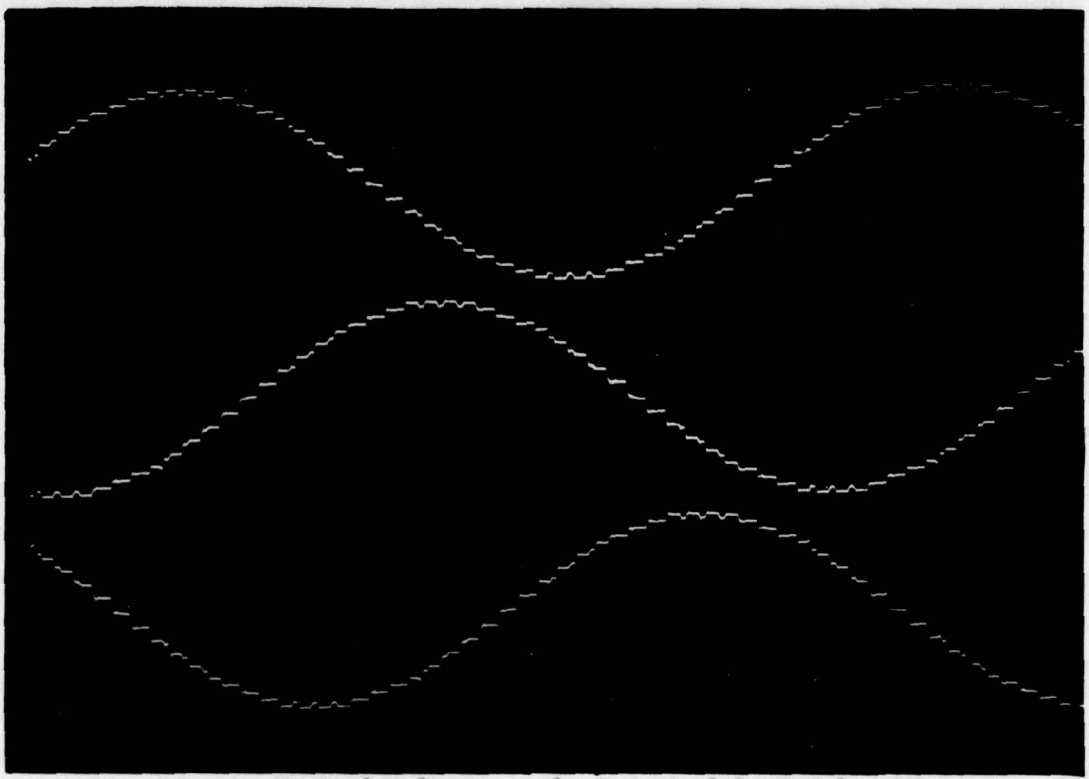


Figure 2-12. Line-to-Neutral Voltages at the Output of the Triplen Attenuator, TDH=4.2%

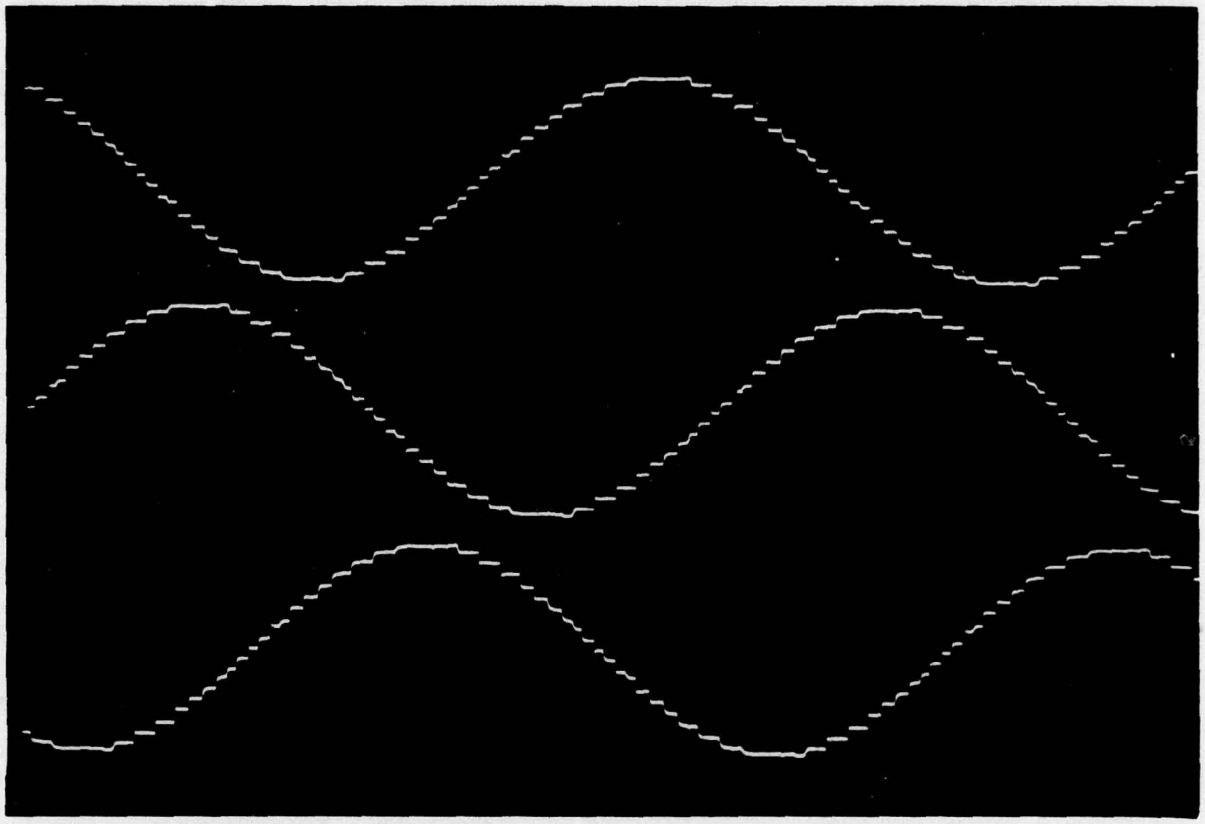


Figure 2-13. Inverter Unfiltered, Three-Phase, Line-to-Line Voltages

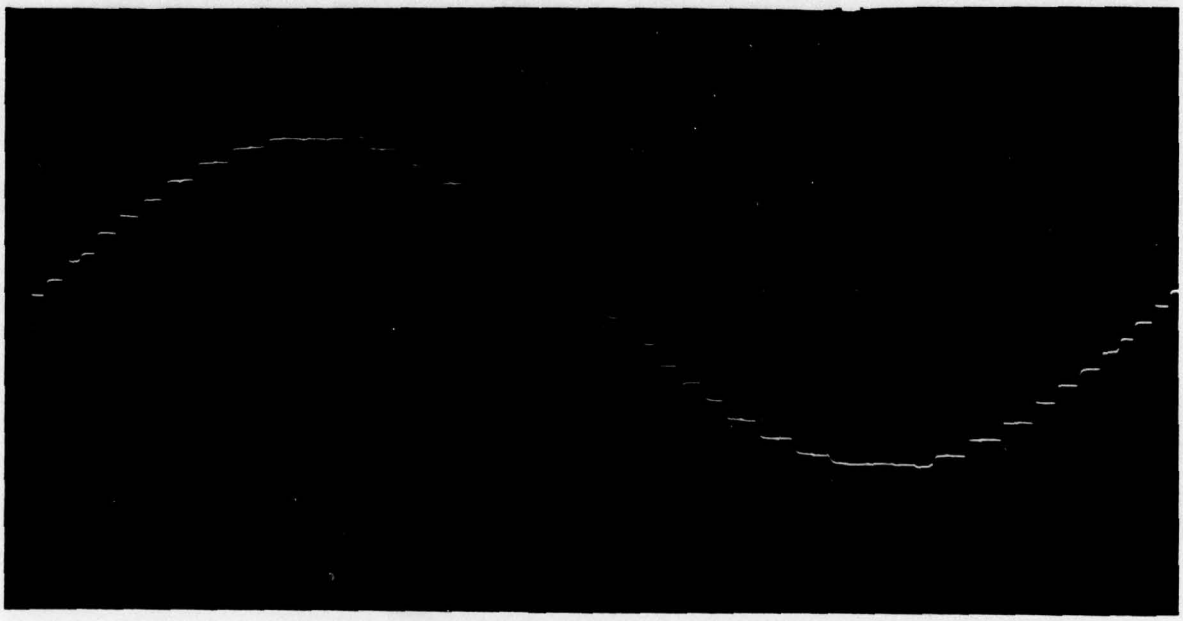


Figure 2-14. Unfiltered, Line-to-Line Voltage

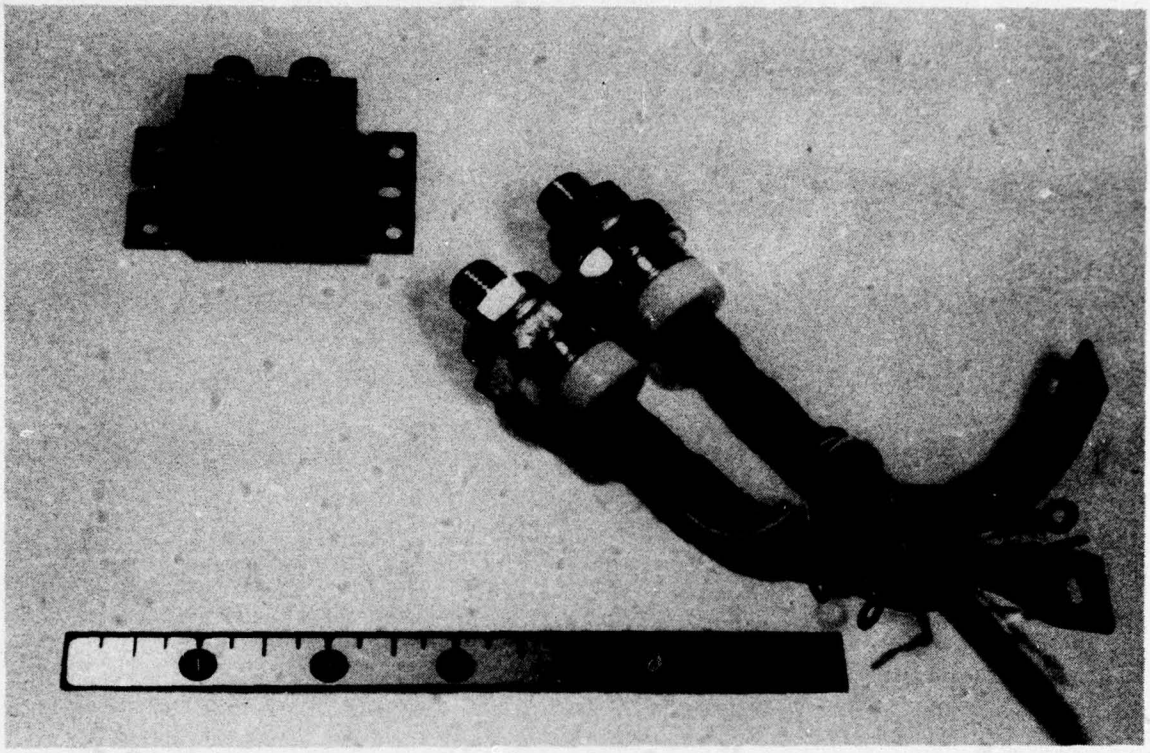


Figure 2-15. Comparison of Stud-Mounted Thyristors with Insulated Base Plate Type

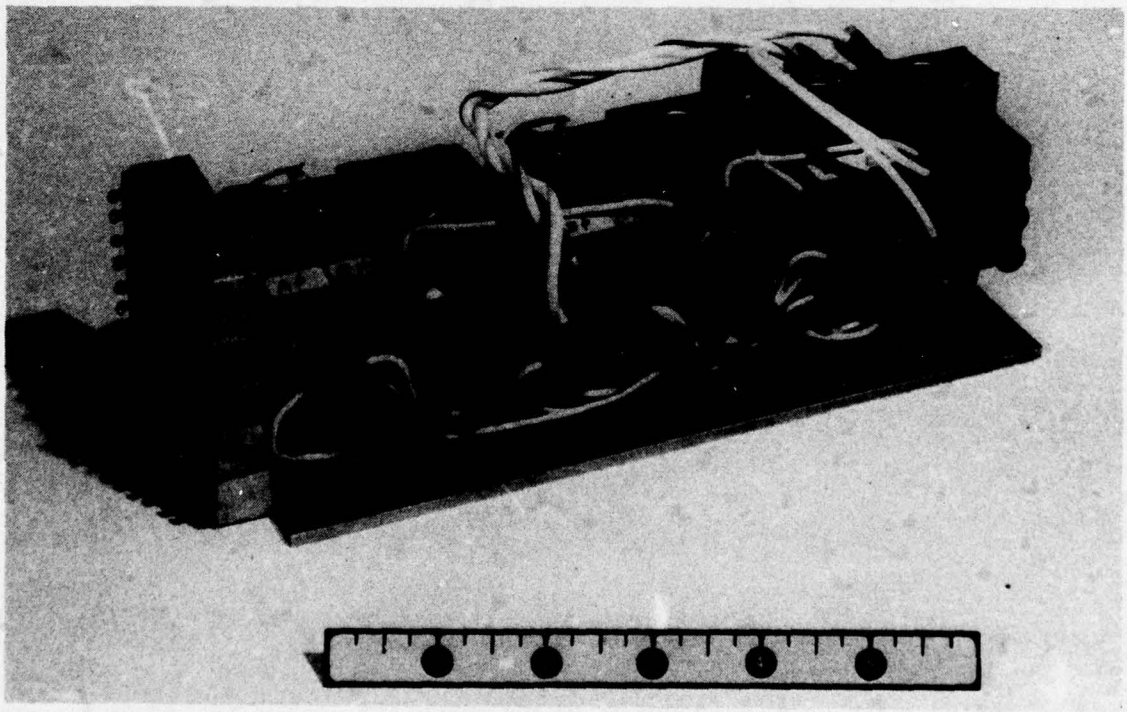


Figure 2-16. T^+, T^-, and "Center" Thyristors Assembled on the Sink

Figure 2-16 shows the assembly of the T^+, T^- and "center" thyristors on a heat sink structure. Installation of the thyristors requires only a screwdriver for bolting the copper flanges to the heat sink and for connecting the power leads.

Assembly of one of the two sets of step selector thyristors is shown in Figure 2-17 and a typical step commutation transistor assembly is shown in Figure 2-18. Four transistor assemblies are required in the inverter. Figure 2-19 shows the complete inverter power switch assembly mounted on a finned aluminum heat sink.

2.1.2.2 Rectifier – Input Filter

A schematic diagram of the rectifier and input filter are shown in Figure 2-8. The rectifier is a three-phase, two-way bridge circuit that converts the 1,550 Hz alternator voltages to dc. The input filter consists of two 125 μF capacitors; one connected from the plus dc line-to-neutral and the other connected from the minus dc line-to-neutral.

2.1.2.3 Output Filter

The output filter consists of three 20 μF capacitors. One capacitor is connected from line-to-neutral for each phase at the inverter output.

2.1.2.4 Drivers

A top view of the completed breadboard inverter is shown in Figure 2-20. On the right side of the photograph is shown the mounting of the driver, timing and protection circuits. Figure 2-21 is a photograph of a typical driver circuit card.

The driver circuits are transformer isolated and supply current to each transistor or SCR for the entire period it is to conduct. The principle used is that of gated, rectified RF. TTL NOR gates control the output of each power oscillator. The power input for the oscillators is in the form of constant current. Each thyristor gate drive or transistor base drive circuit is basically a square wave amplifier that is controlled by an output from the memory timing circuit. Figure 2-22 is a schematic diagram of a typical drive circuit. There are six drive circuits on each printed circuit board.

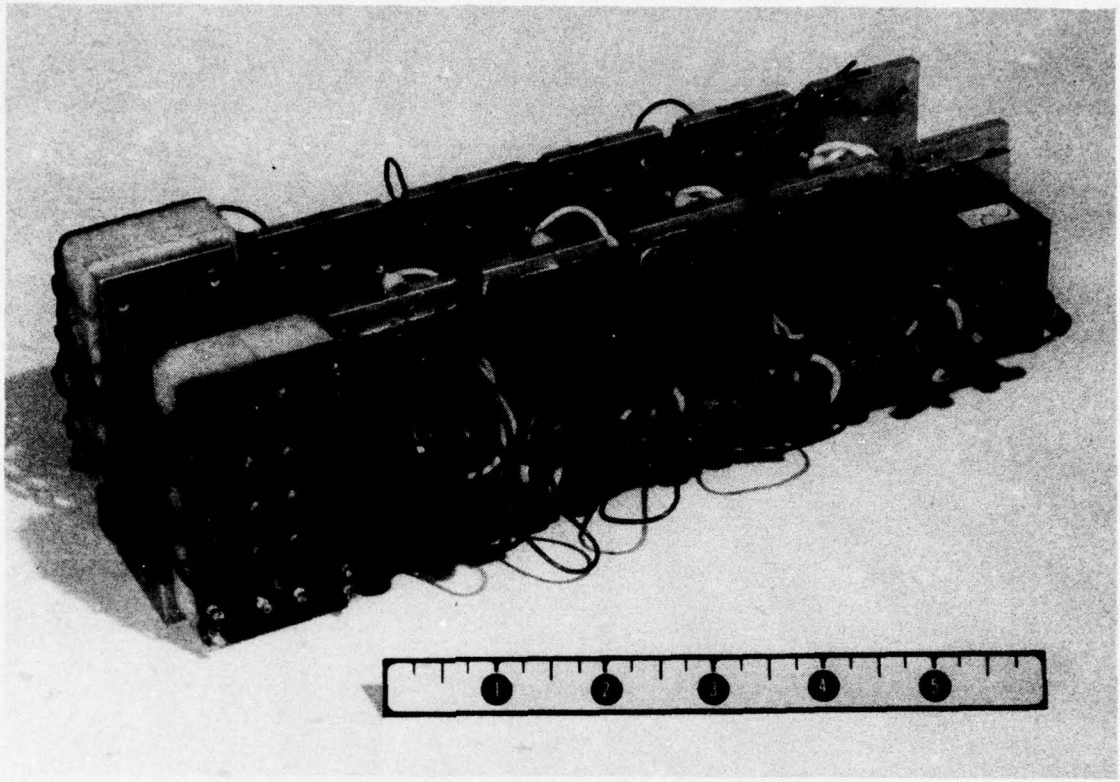


Figure 2-17. Step-Selector Thyristor Assembly

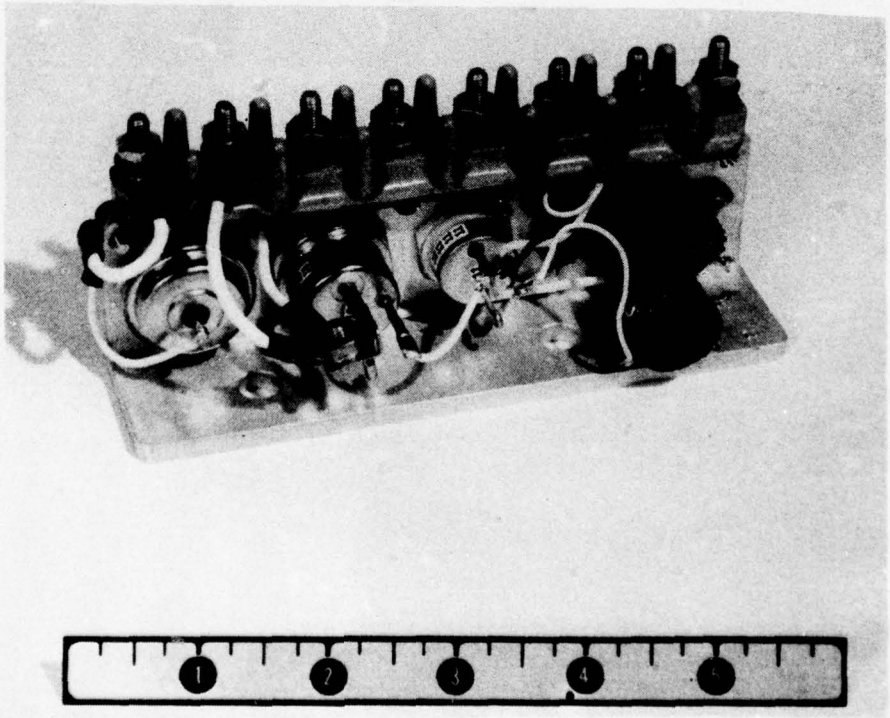


Figure 2-18. Step Commutation Transistor Assembly

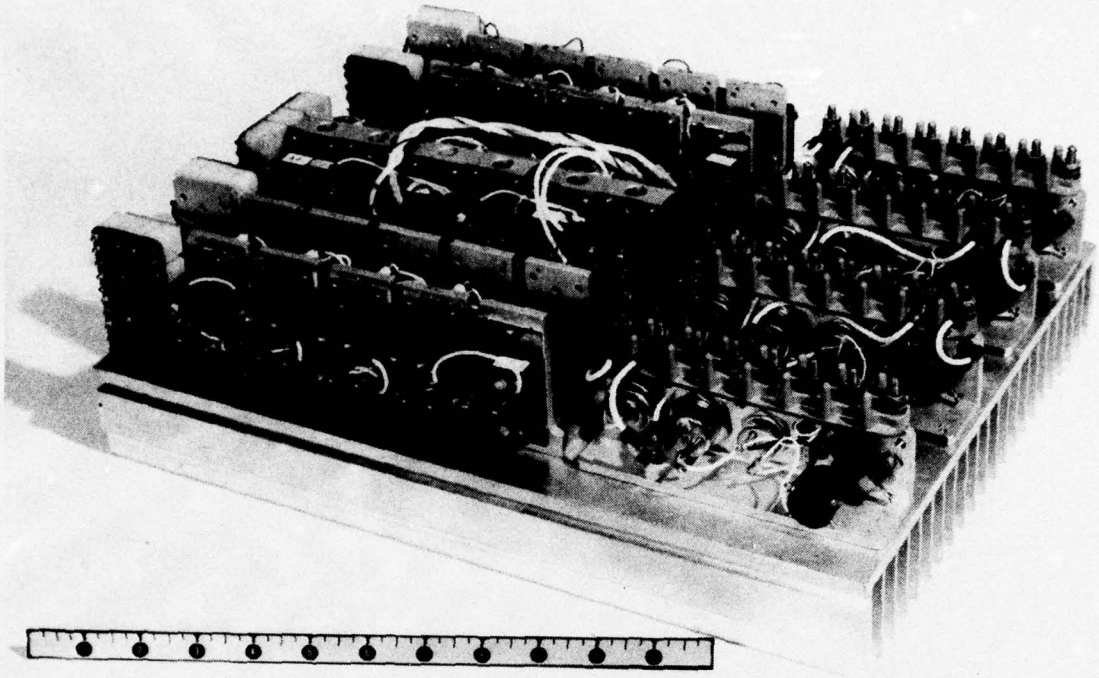


Figure 2-19. Complete Inverter Power Switch Assembly

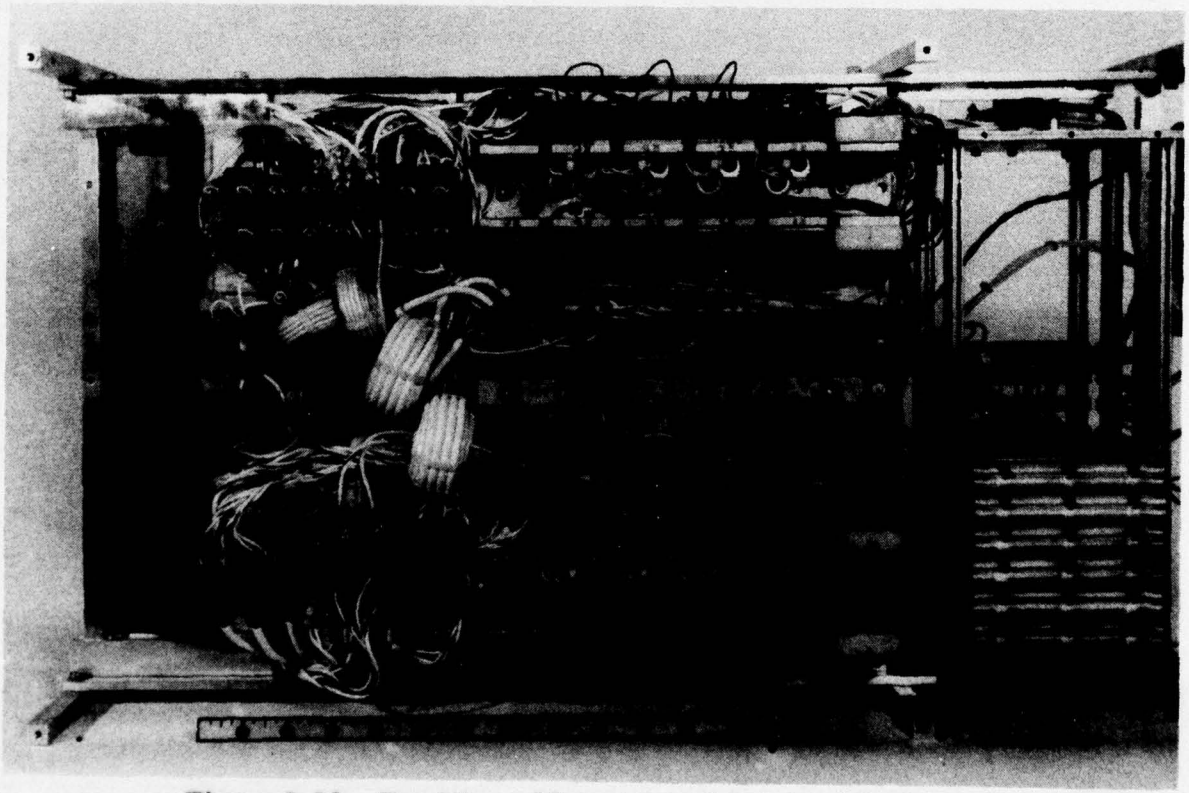


Figure 2-20. Top View of Inverter and Trigger Electronics

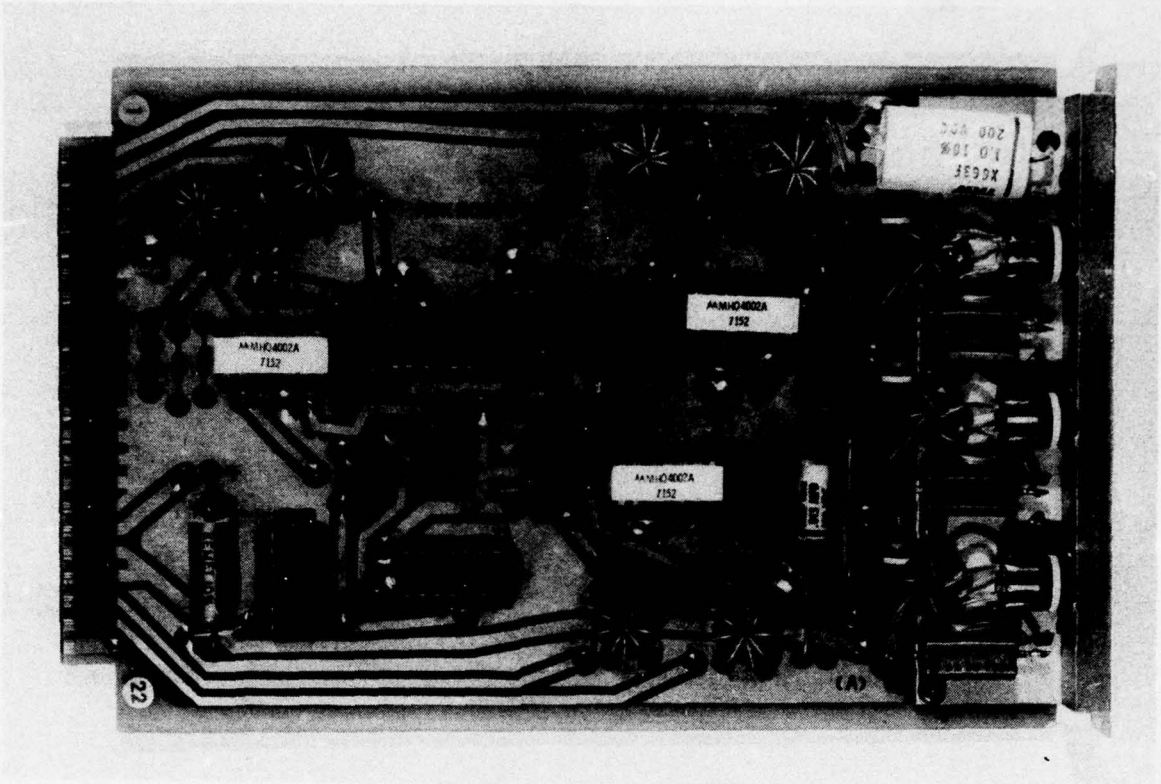


Figure 2-21. Six Driver Circuits

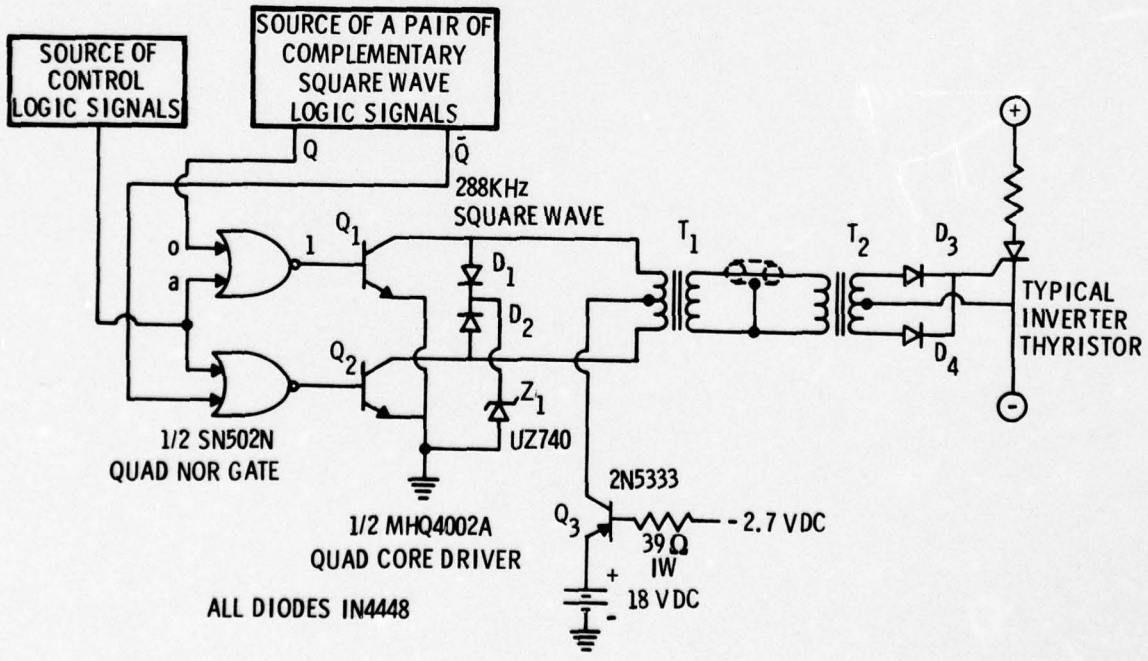


Figure 2-22. Thyristor Gate Drive Circuit

Complementary square wave voltages Q and $\overline{Q}$ at a frequency of 288 kHz is derived from the memory timing circuit. Signal Q is applied to one input of a NOR gate and $\overline{Q}$ is applied to one input of another NOR gate, as shown in Figure 2-22. The second input of each NOR gate is controlled by a thyristor firing signal in the memory timing circuit. The output circuit of each NOR gate is connected to the base of one of two transistors (Q_1, Q_2) connected in a push-pull configuration in the primary of transformer T_1. Logic state 0 on each NOR gate input will produce a logic state at the output and drive one of the push-pull transistors. When a logic 0 signal is present, transistors Q_1 and Q_2 are driven by a 288 kHz square wave current which is amplified, fed through transformers T_1 and T_2 and rectified by diodes D_3 and D_4 to provide gate drive current for the thyristor.

Transistor Q_3 functions as an impedance that gives the dc power source the characteristics of a current source. Diodes D_1 and D_2 and zener diode Z_1, provide a clamp circuit for the collectors of transistors Q_1 and Q_2 to protect them from excessive voltage spikes.

Trigger noise and crosstalk is minimized by making T_1 and T_2 small, high frequency ferrite toroidal transformers with primary-to-secondary capacitance of approximately 2 to 3 x 10^{-12} farads. Coaxial or twisted-pair cable is used with transformers on the driven ends and also on the driven device ends. This high degree of isolation, in addition to minimizing noise, ensures protection of the waveform generator and drivers from damage caused by failures in the power switch assembly.

2.1.2.5. Memory Timing Circuit

The inverter is a programmed waveform device; each trigger pulse is synchronized with a crystal controlled counter. An inherent invantage of this type of control is that the inverter output does not contain any phase or frequency modulation. Figure 2-23 shows the memory timing circuit board.

The waveform generator is constructed with five-volt, medium-power, TTL integrated circuits. A schematic diagram is shown in Figure 2-24. The output of a crystal oscillator is divided to produce 120 counts per 16.67 ms (for 60 Hz) or 2.50 ms (for 400 Hz). The counter, with seven-bit output and an eighth bit for frequency, parallel addresses eight read only memories (ROM). Each ROM has a four-bit output word length. Thus, each of the 120 counts produces a corresponding 32-bit word. Each power switching device, transistor or SCR, or antiparallel pair of devices is controlled by one bit from the 32-bit word.

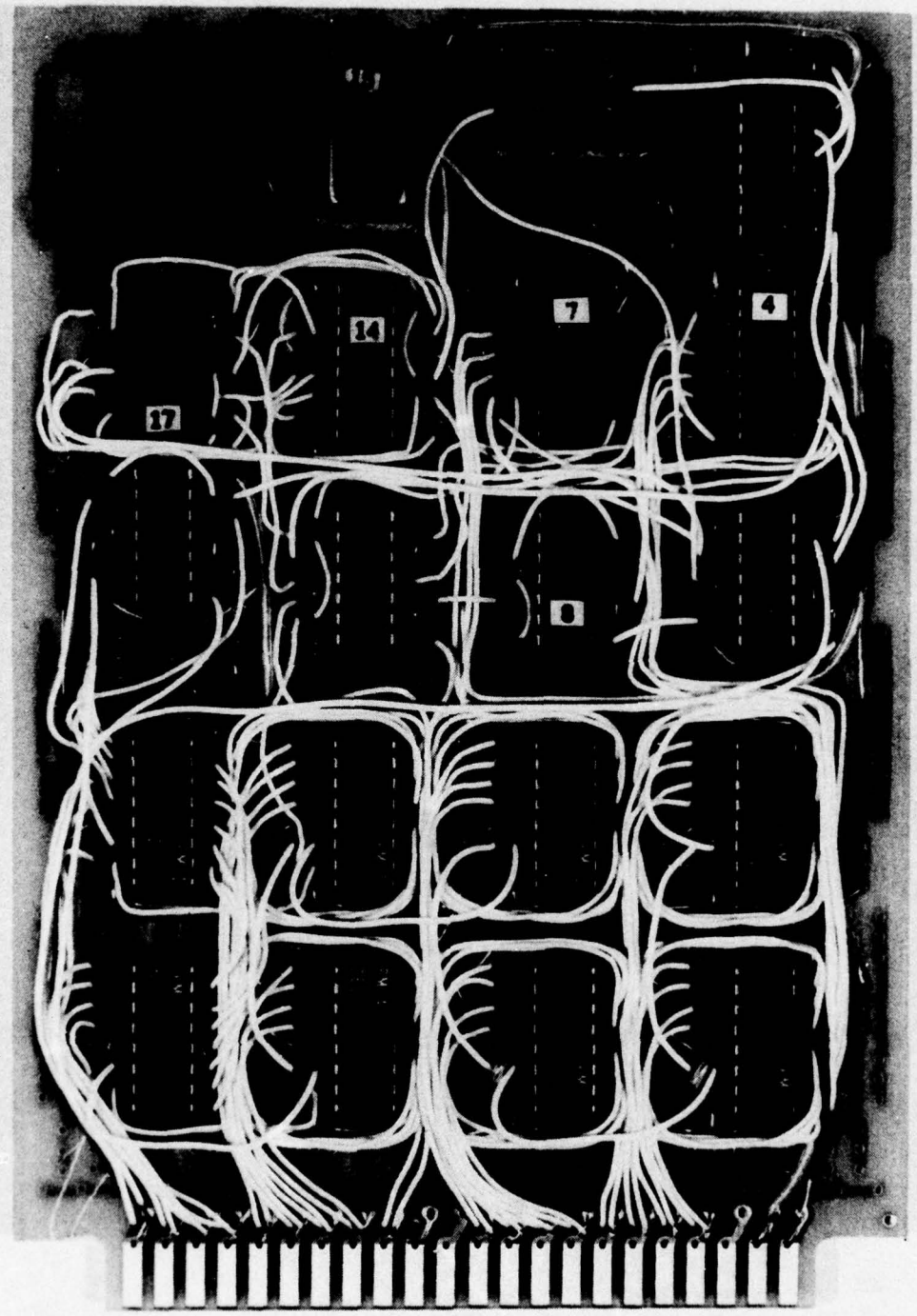


Figure 2-23. Memory Timing Circuit

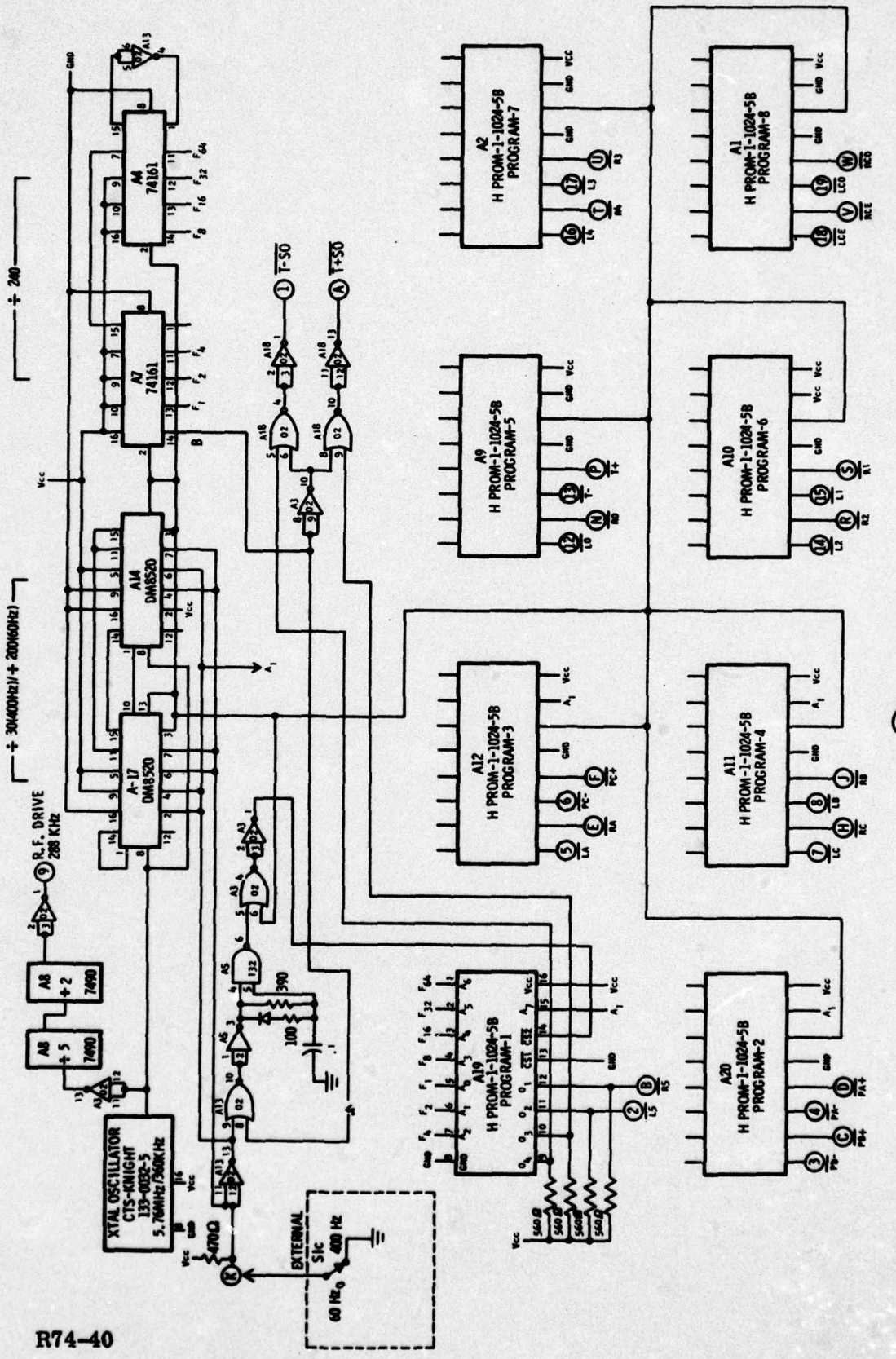


Figure 2-24. Memory Timing Circuit

This method of waveform generation, where trigger drives are decoded directly from a binary digital divider, is inherently simple and reliable. The breadboard inverter uses several IC packages: a crystal oscillator, two module-N dividers, a decade counter, two synchronous four-bit binary counters, several gates, and eight programmable ROM's. A larger scale of integration would simplify the waveform generator substantially. Commercial temperature range logic is used, but -55°C to +125°C logic, which is pin for pin interchangeable, is readily available.

2.1.2.6 Protection

Protection is employed against all causes of di/dt and dv/dt, as well as instantaneous surges of voltage and current in the power switch assembly. Nonsaturating inductors in critical areas limit the rate of rise of SCR current to safe values. These inductors also function with RC snubbers to control the rate of rise of reapplied forward voltage. The size of the alternator, its saturation characteristics, and the sizing of the input filter confine currents and voltages to limits which are easily tolerated by the SCR's. The power transistors need additional protection because their peak energy absorption capability is relatively small. Surge power zener diodes clamp V_{ce}; I_c sensors cut the base drive before I_c gets too high. Transistor drive is restored immediately upon the clearing of the fault. When the average output current from the alternator gets too large, it is limited by a reduction in field current. The protection circuit card is shown in Figure 2-25.

2.1.2.7 Alternator Field Control

A field control regulator is used on the alternator to regulate the inverter's output voltage and current. Figure 2-26 is a photograph of this circuit. Pulse frequency modulation of current from the 28-volt battery source is used to control field current. The feedback is accomplished in a single compensated loop. Two variables, the average value of the full-wave rectified, three-phase inverter output voltage and the same function of the alternator output current, are compounded to give close load regulation. Current limiting is obtained solely from sensing the latter variable. The regulator is fast relative to the time constant of the alternator field, but no attempt is made to force the field. The regulator is self-contained and independent of the inverter and its auxiliary power supply.

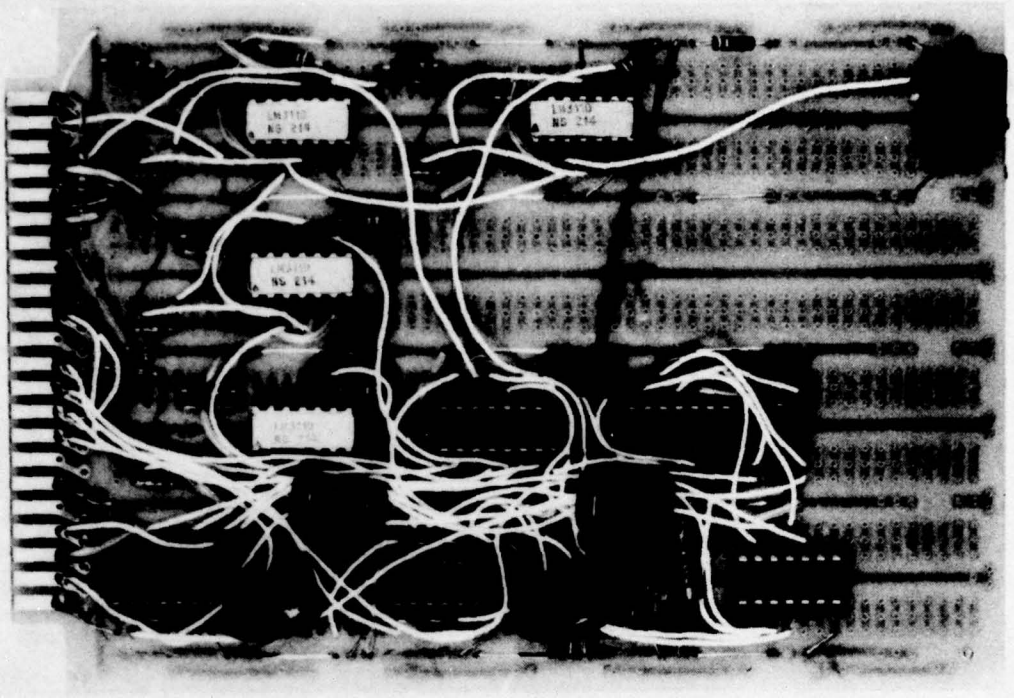


Figure 2-25. Protection Circuits

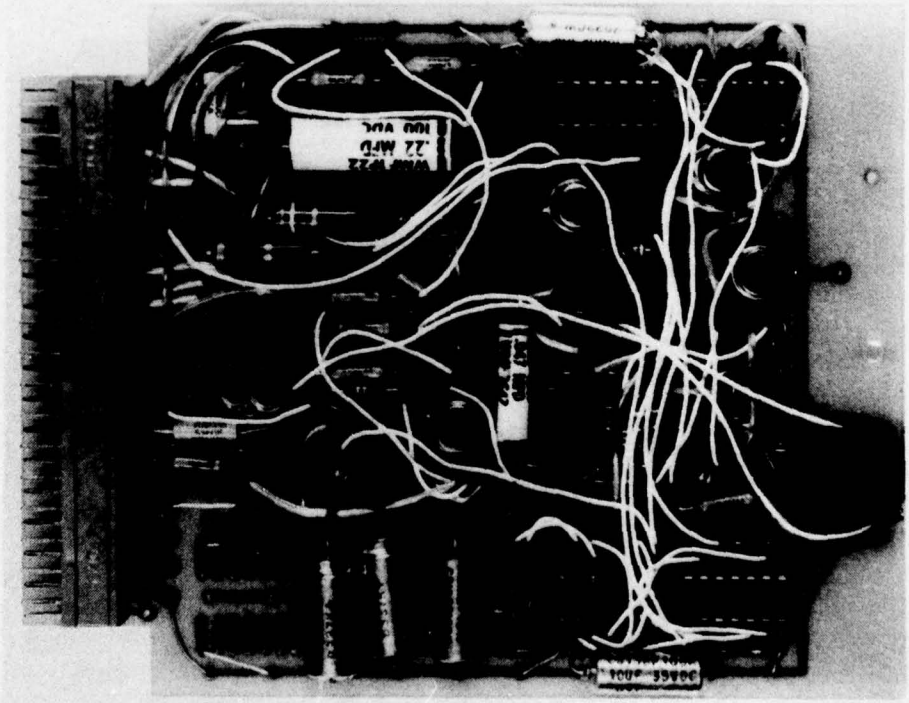


Figure 2-26. Alternator Field Control Circuit

2.1.2.8 Auxiliary Power Supply

The auxiliary power supply operates from an input voltage of 24-30 volts dc and provides +18 volts dc, -2.7 volts dc for the driver circuits, and +5 volts dc for the memory timing circuit. These output voltages are regulated to better than ± 1% and have less than 0.5% ripple. The power supply weighs less than 4 lb and has an efficiency of 82%.

Test results for Item No. 0001 are compiled on pages 1-14 of Volume II of this report.

2.2 MODIFICATION OF CONVERTER (ITEM No. 0003)

The contract work statement required modifying the Frequency Converter Unit furnished as Item No. 0001, to comply with the electrical performance criteria of Attachment No. 3, except that the motor starting performance specified in Paragraph 3.24.4 therein shall not be provided. Item No. 0003 is required to produce the following output voltages and frequencies;

- Three-phase, four-wire at 60 Hz, 120 volts line-to-neutral and 208 volts line-to-line (120/208 volts) at 10 kW, 0.8 power factor.
- Three-phase, four-wire, 400 Hz, 120/208 volts at 10 kW, 0.8 PF.
- Single-phase, three-wire, 60 Hz, 120 volts line-to-neutral and 240 volts line-to-line (120/208 volts) at 10 kW, 0.8 PF
- Single-phase, three-wire, 400 Hz, 120/240 volts at 10 kW, 0.8 PF.
- Single-phase, two-wire, 60 Hz, 120 volts line-to-line at 10 kW, 0.8 PF.
- Single-phase, two-wire, 400 Hz, 120 volts line-to-line at 10 kW, 0.8 PF.

2.2.1 PRODUCING SINGLE-PHASE POWER

The Delco breadboard inverter inherently produces three-phase power. Single-phase power is also available up to the rating of the breadboard, but with one qualification. The rating of the output zig-zag transformer determines the magnitude of the unbalance or single-phase loads that are acceptable. For balanced three-phase loads, the zig-zag transformer is essentially unloaded and its primary function is to provide the neutral connection for a four-wire system. The transformer maintains equal currents in the windings for any load unbalance conditions. The result is current flow in all phases of the inverter, even though there may be a load on only one of the line-to-neutral phases.

This action helps to maintain voltage balance across the three phases. If one phase is leading or lagging, the autotransformer will automatically feed flux to the leg corresponding to that phase from the other two legs, thus restoring the proper phase relationship. The vector relationships between line currents and the line-to-neutral voltages for a single-phase load are illustrated in Figure 2-27. The current in line A is 2/3 the load current and is in phase with the line-to-neutral voltage. The current in line B is 1/3 the load current and lags the phase voltage by 60°. Line C current is also 1/3 the load current and leads the phase voltage by 60°. Two-thirds of the load power is delivered by line A and 1/6 of the power is delivered each by lines B and C. Line A carries twice the current for rated single-phase loads compared to rated three-phase loads.

Single-phase, two-wire loading of the Delco inverter can be achieved without circuit modification. The allowable magnitude of the unbalanced load is determined primarily by the volt-ampere rating of the zig-zag output transformer. But single-phase, 120/240 Vrms, three-wire power is not inherently available. Several schemes were investigated that produced 120/240 Vrms power, balanced or unbalanced. These are as follows:

- Method 1: Seven-winding zig-zag transformers that provide output connections for three-phase, single-phase, two-wire, or single-phase, three-wire, as illustrated in Figures 2-28, 29, and 30.
- Method 2: Eight-winding zig-zag transformers, with connections shown in Figures 2-31, 32 and 33.
- Method 3: Six-winding zig-zag transformers with auxiliary transformer a, shown in Figure 2-34.
- Method 4: Six-winding zig-zag transformer with auxiliary transformer b, illustrated in Figure 2-35.
- Method 5: Zig-Zag to delta connection, as illustrated in Figures 2-36 and 2-37. Figure 2-36 shows the windings of the output transformer connected in a zig-zag configuration to produce three-phase and single-phase, two-wire power. The output transformer is connected in a delta configuration, as shown in Figure 2-37, to produce single-phase, 120/240 V rms single-phase power.
- Method 6: Single-phase autotransformer connected line-to-line, as shown in Figure 2-38. This transformer can be tapped to produce 120 V two-wire or 120/240 three-wire power, and it can be designed to operate efficiently at 60 Hz or 400 Hz.

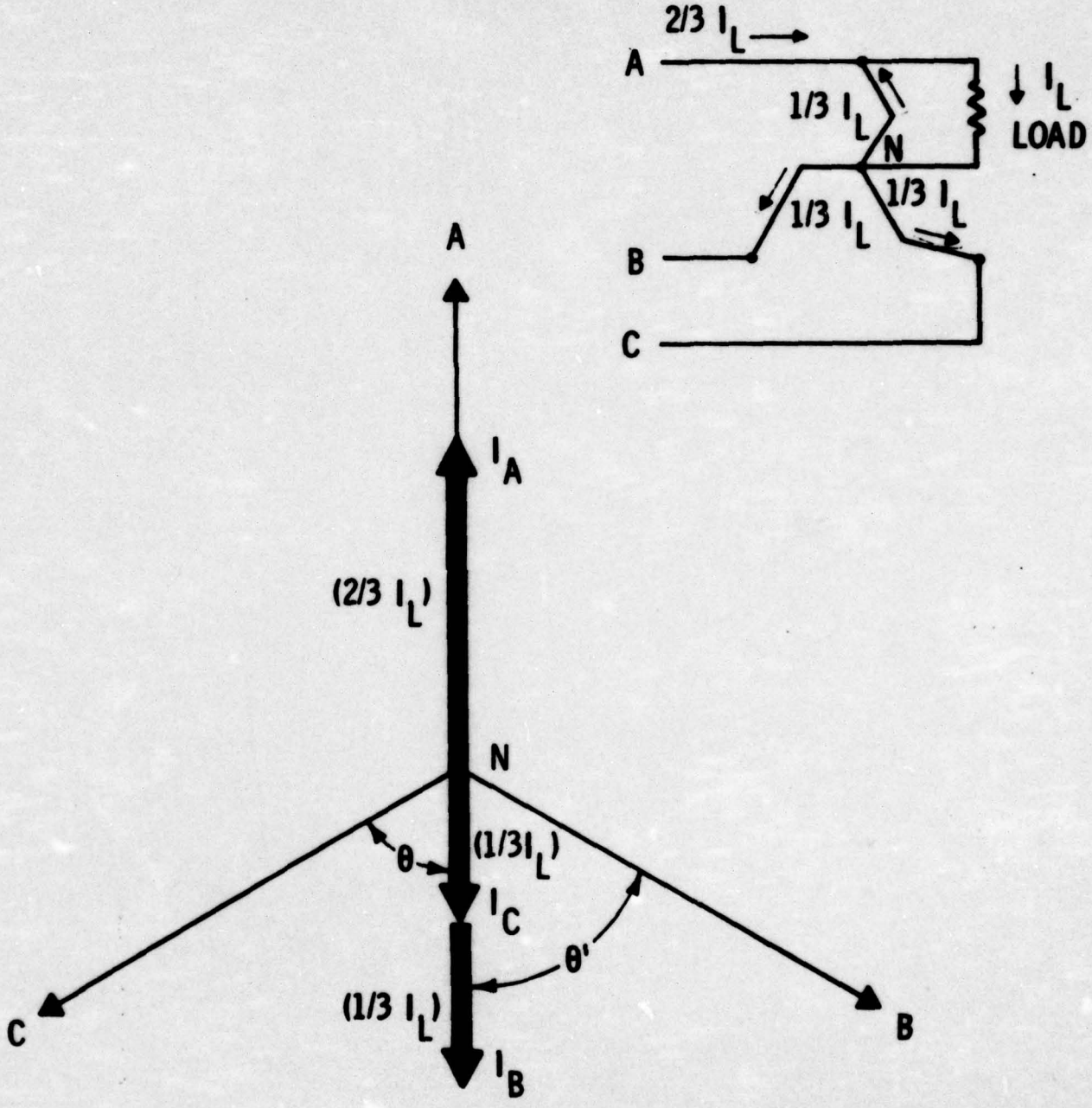


Figure 2-27. Vector Relationships Between Line Currents and Line-to-Neutral Voltages for a Single-Phase Load Connected to the Inverter Output Zig-Zag Transformer

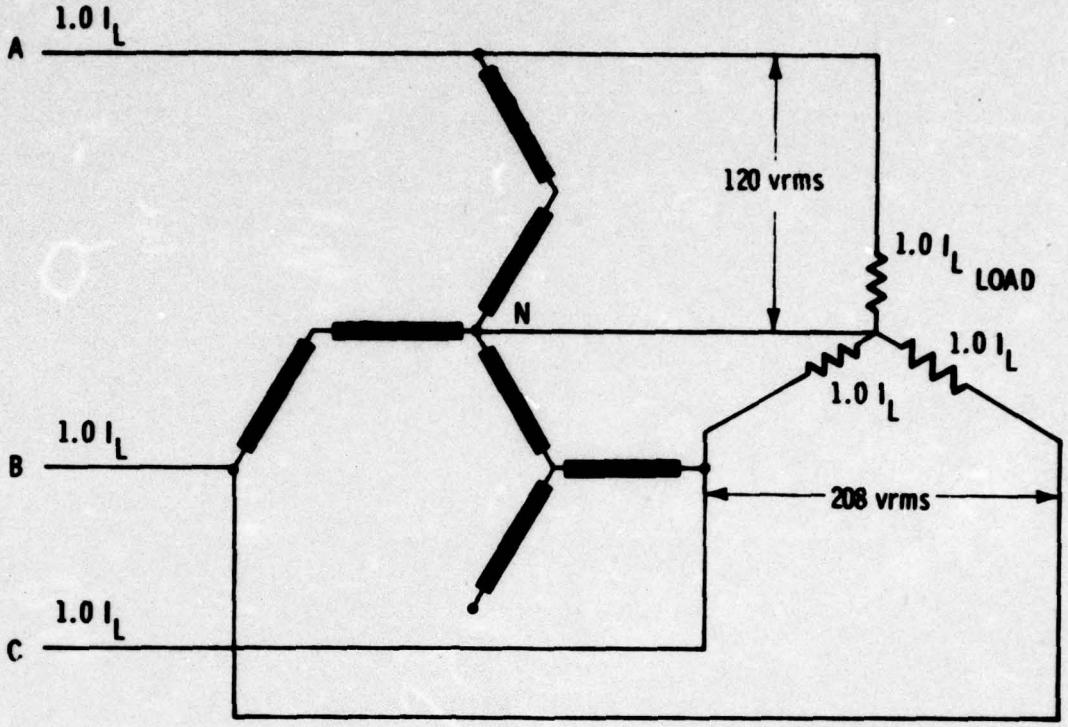


Figure 2-28. Seven Winding Zig-Zag Transformer Three-Phase Load Connection

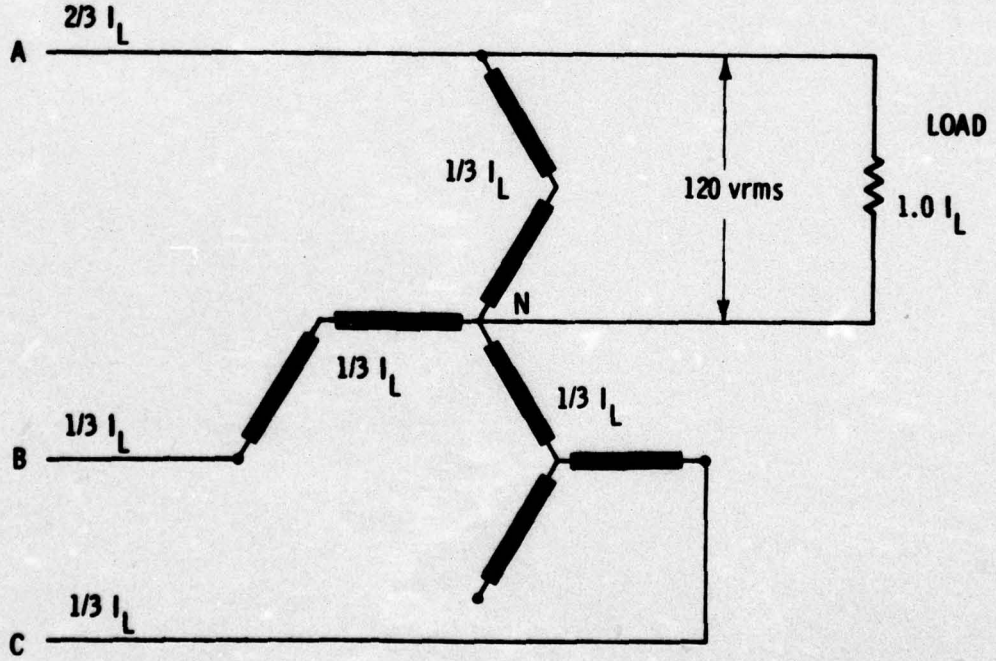


Figure 2-29. Seven Winding Zig-Zag Transformer Single-Phase, Two-Wire Load Connection

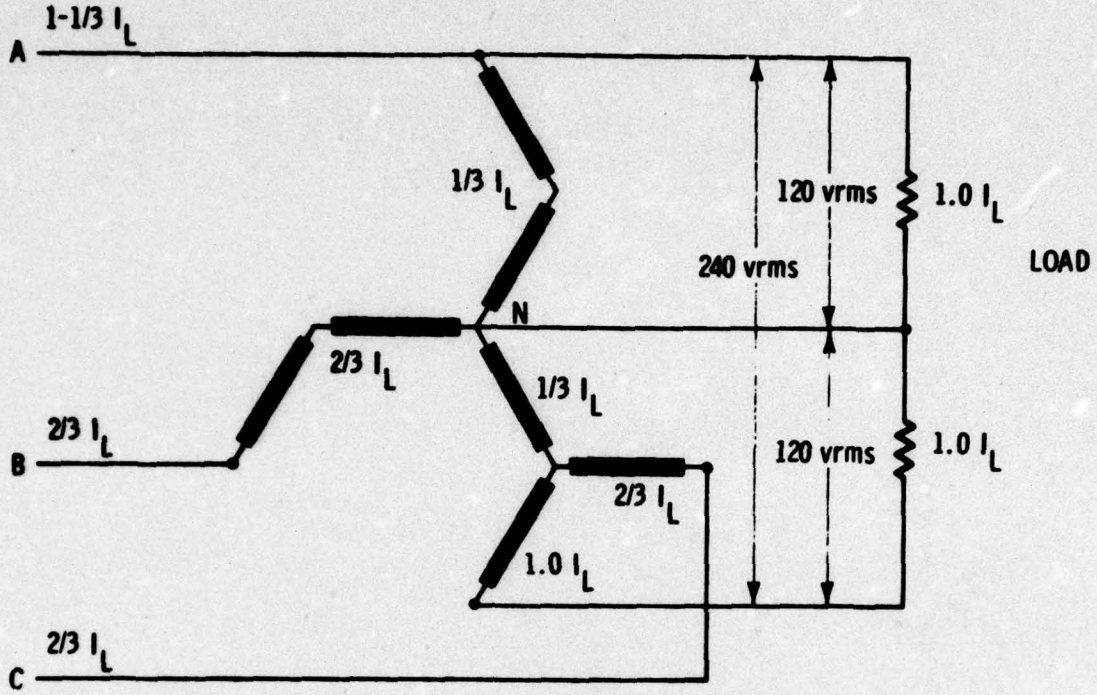


Figure 2-30. Seven Winding Zig-Zag Transformer Single-Phase, Three-Wire Load Connection

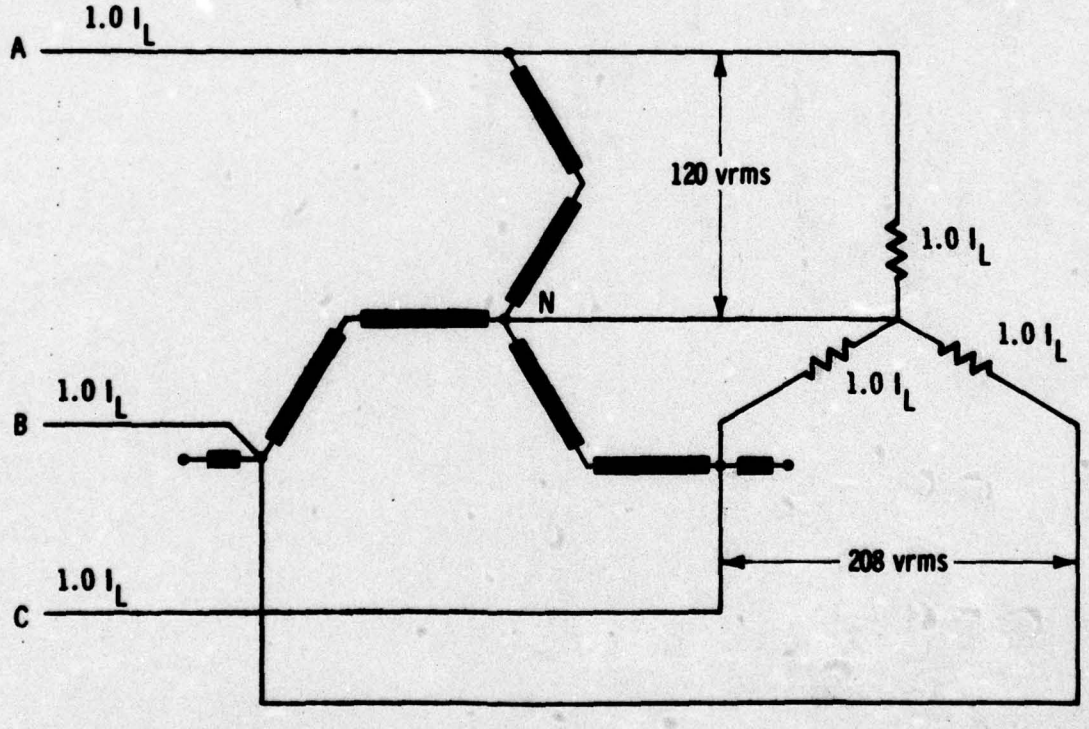


Figure 2-31. Eight Winding Zig-Zag Transformer Three-Phase Load Connection

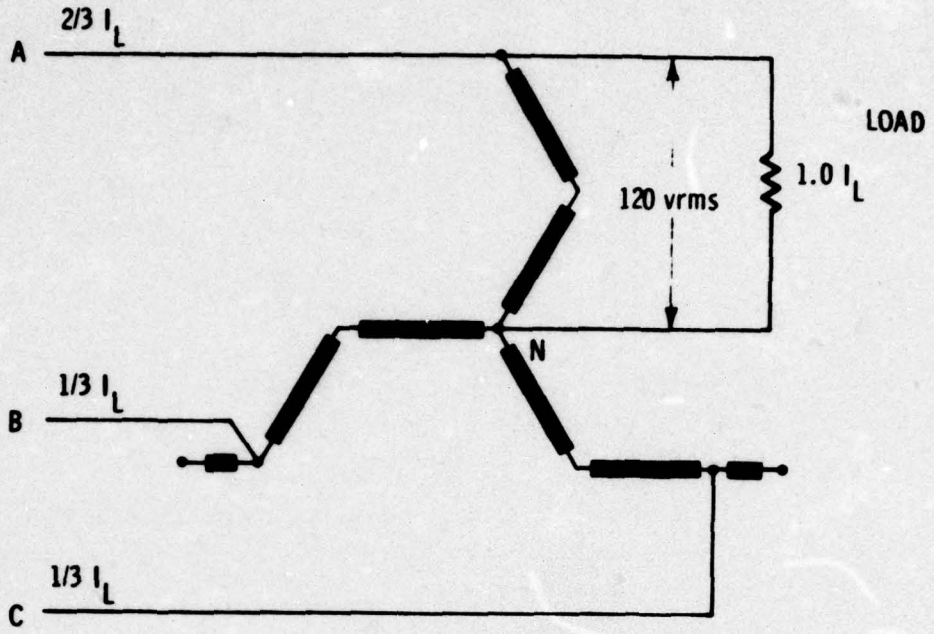


Figure 2-32. Eight Winding Zig-Zag Transformer Single-Phase, Two-Wire Connection

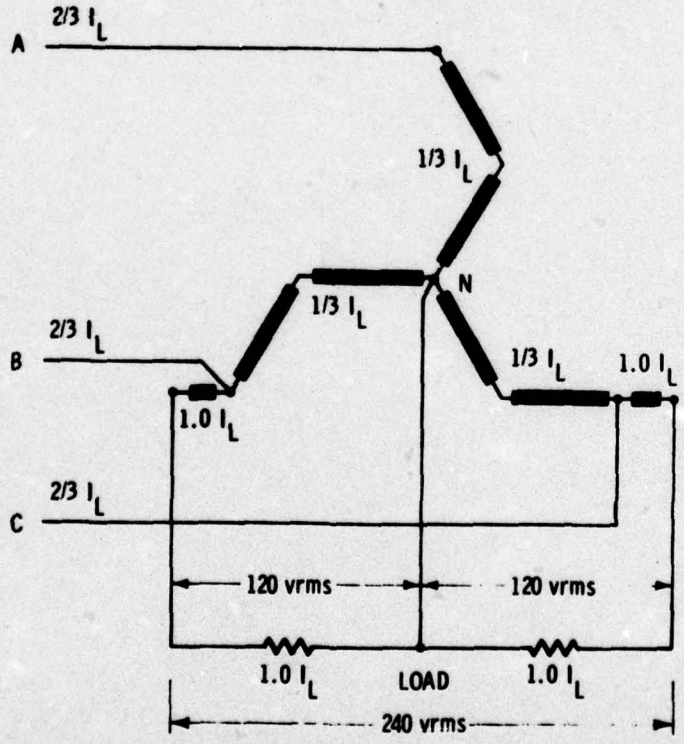


Figure 2-33. Eight Winding Zig-Zag Transformer Single-Phase, Three-Wire Winding

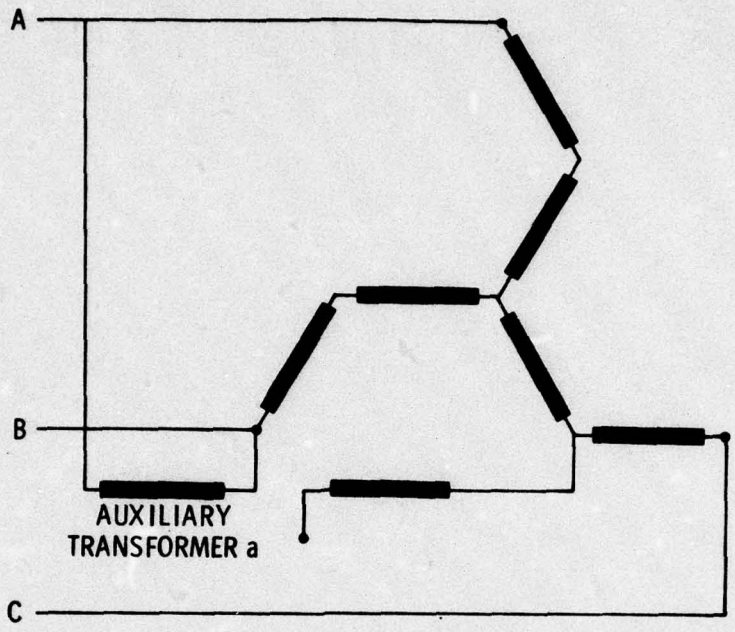


Figure 2-34. Six Winding Zig-Zag Transformer with Auxiliary Transformer a

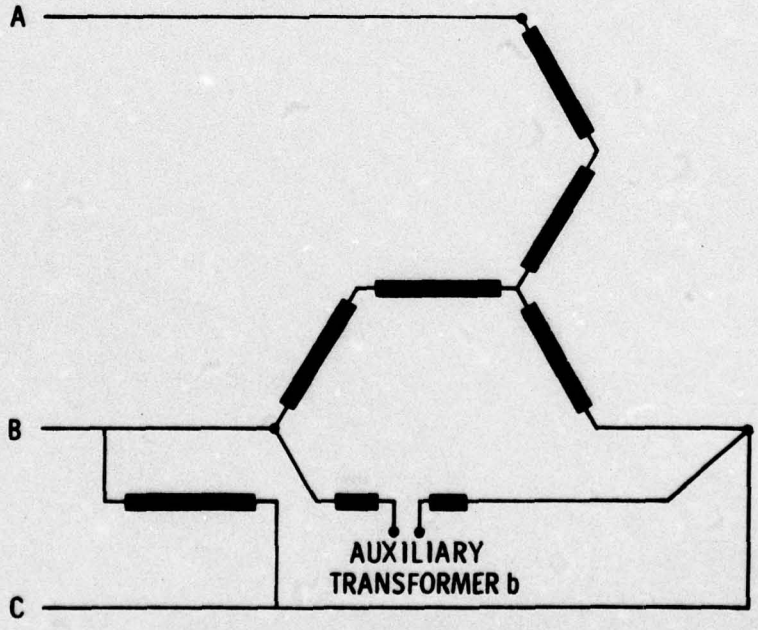


Figure 2-35. Six Winding Zig-Zag Transformer with Auxiliary Transformer b

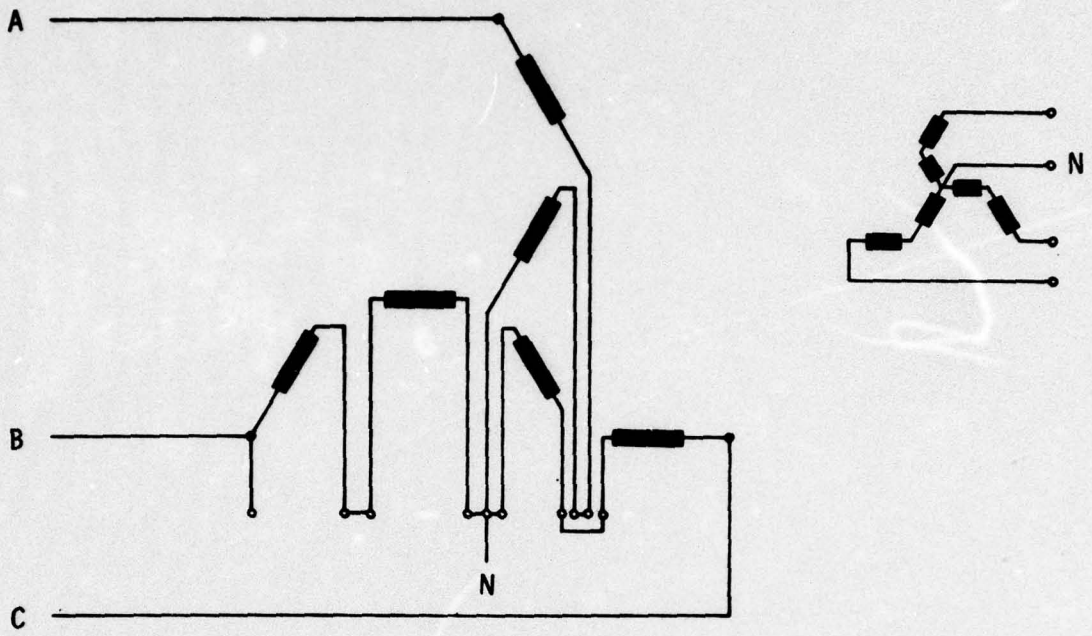


Figure 2-36. Line Balancing Transformer Connected in Zig-Zag Configuration for Three-Phase or Single-Phase Two-Wire Operation

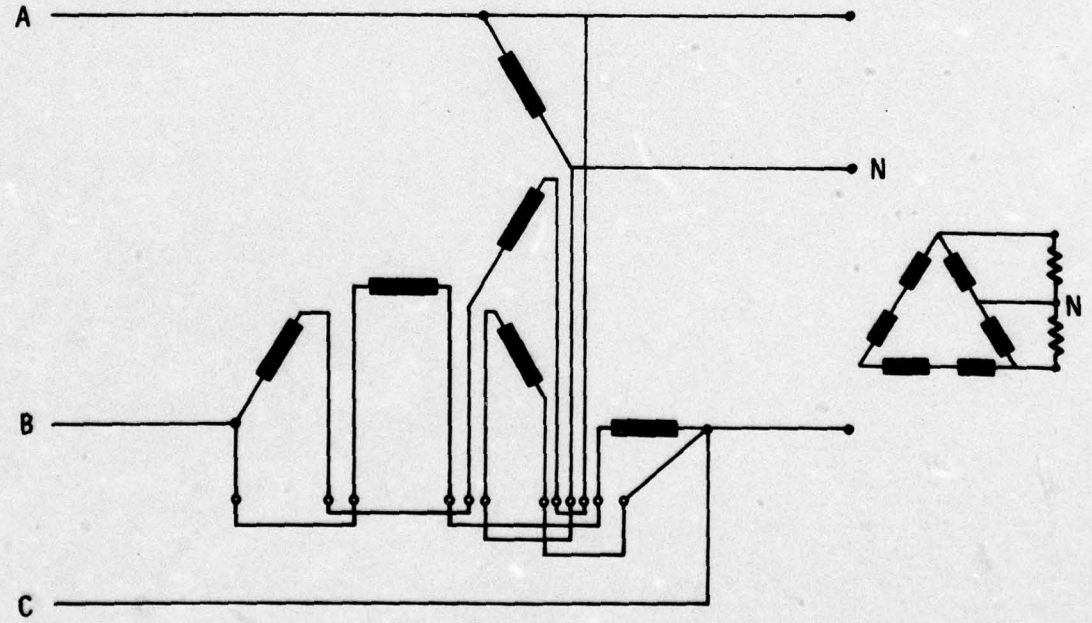


Figure 2-37. Line Balancing Transformer Connected in Delta Configuration for Single-Phase, Three-Wire Operation

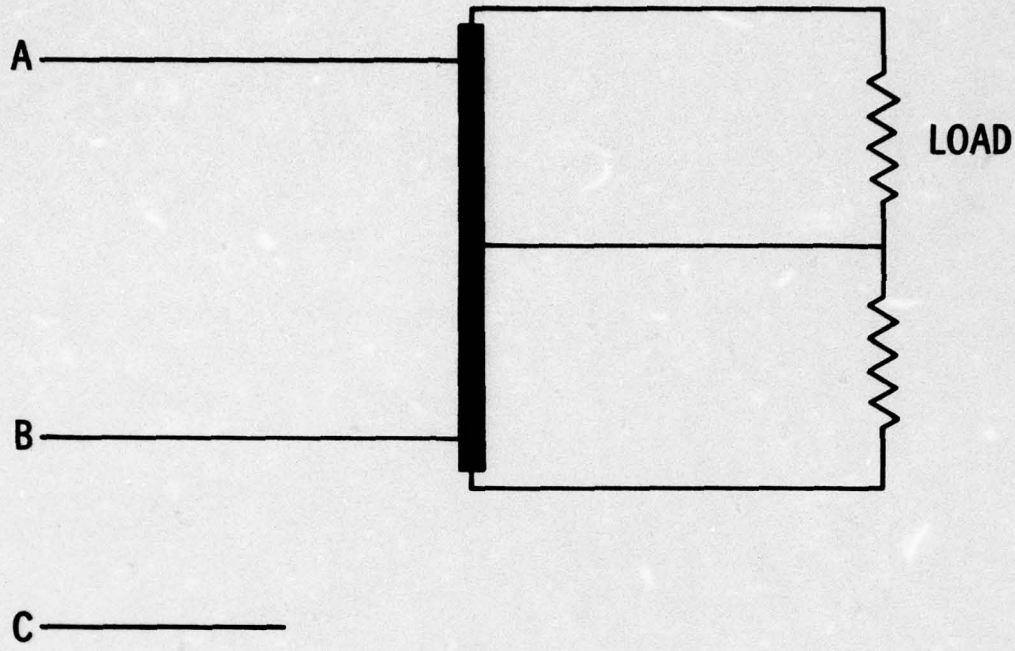


Figure 2-38. Multi-Tapped, Single-Phase Autotransformer Connected Line-to-Line at the Output of the Frequency Converter

2.2.2 EFFECTS OF SINGLE-PHASE LOADS

For three-phase operation with balanced loads, the ripple frequency of the dc current into the Delco inverter is predominantly 1,200 Hz with a ripple magnitude of about 50%. When the inverter energizes a single-phase load, the input current ripple frequency becomes predominantly 800 Hz with a ripple magnitude of about 100%. Because of this change in input characteristics of the inverter, single-phase operation has an influence on the design of the input filter. Analysis and experimentation were required to determine the effects of single-phase operation on the high-speed alternator output and filter weight.

2.2.3 OUTPUT FILTER CONSIDERATIONS

The voltage waveforms at the output of the switching section of the Delco inverter are designed for minimum total harmonic content. In addition, those harmonics that are one percent or higher are arranged to cluster about the 40th harmonic. The purpose of this waveform design is to minimize energy storage in the output filter.

Tuned, attenuating, filter circuits are avoided because resonance can increase total harmonic content and because they are sensitive to load magnitude and power factor. Analysis and experimentation were required to determine the influence of single-phase, three-wire output transformer circuits on output filter design.

The technical effort was organized on the basis of accomplishing the following tasks:

- Task 1: Methods of investigation, transformer analysis, and design. Because the inverter is a breadboard, design the output transformer for free connection cooling rather than turbine air flow cooling.
- Task 2: Input filter investigation and design. Filter fabrication and test.
- Task 3: Output filter investigation and design. Filter fabrication and test.
- Task 4: Inverter modification and test for three-phase/single-phase operation.

2.2.4 SUMMARY OF INVESTIGATION

Methods 1-5 in which various configurations of zig-zag transformers were used to provide single-phase, two- and three-wire power proved to be difficult to design, expensive and inefficient compared to Method 6.

When single-phase loads are connected line-to-line, the zig-zag transformer does not handle the unbalance and is essentially unloaded. Our studies and tests indicated that the most efficient method to obtain single-phase power from the Delco inverter is by means of a single-phase autotransformer connected line-to-line.

A schematic diagram of the transformer designed to provide the single-phase voltage connections is shown in Figure 2-39. For 60 Hz operation, lines A and B of the inverter are connected to taps 1 and 4 of the autotransformer. For 400 Hz operation, lines A and B are connected to taps 2 and 3. Schematic diagrams showing the connections of the autotransformer for all single-phase requirements are given in Figures 2-40 through 2-43. The autotransformer weighs 39 pounds and has an efficiency of 97.6%. For three-wire, single-phase operation, data showing voltage unbalance for unbalanced loads are given in Table 2-2.

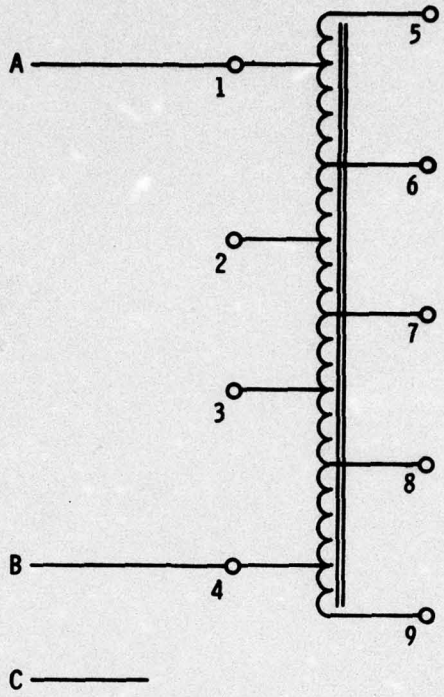
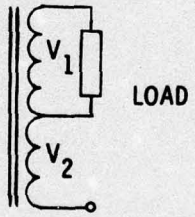


Figure 2-39. Schematic Diagram of the Single-Phase Autotransformer



SINGLE PHASE OUTPUT TRANSFORMER

V_1 (Vrms)	V_2 (Vrms)	LOAD (kW, PF = 0.8)	FREQUENCY (Hz)
121.9	121.9	-	400
121.6	122.2	2.2	400
121.3	122.4	4.4	400
121.4	122.4	5.8	400
120.2	120.2	-	60
120.2	121.4	2.2	60
120.2	122.4	4.4	60
120.4	123.0	5.8	60

Table 2-2. Single-Phase, Three-Wire Voltage Unbalance for Unbalanced Loads

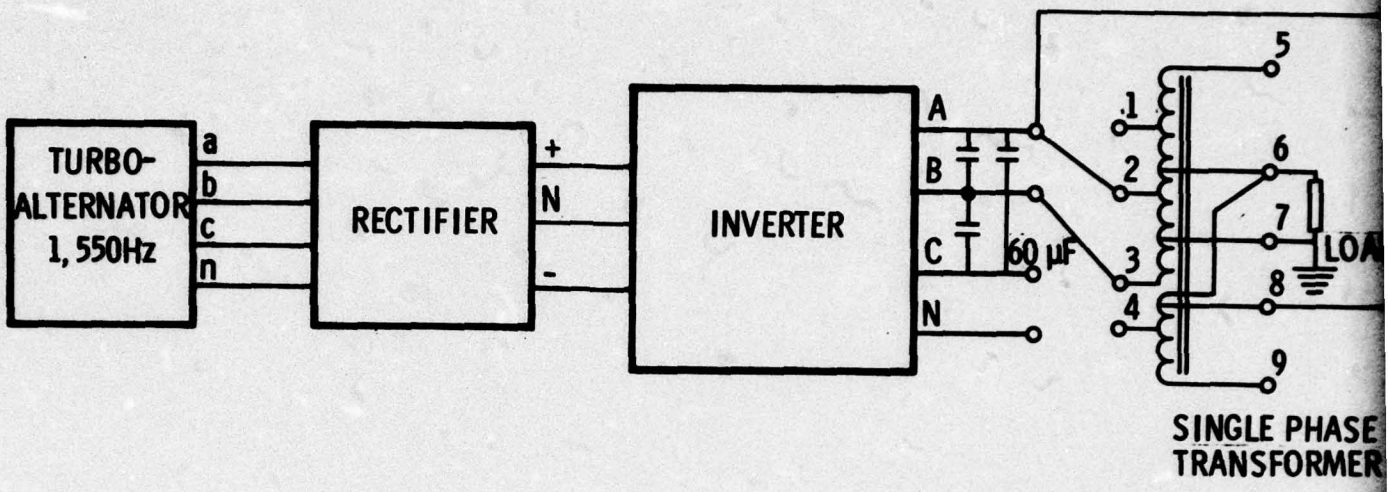


Figure 2-40. Connections for 400 Hz, Single-Phase, Two-Wire Power

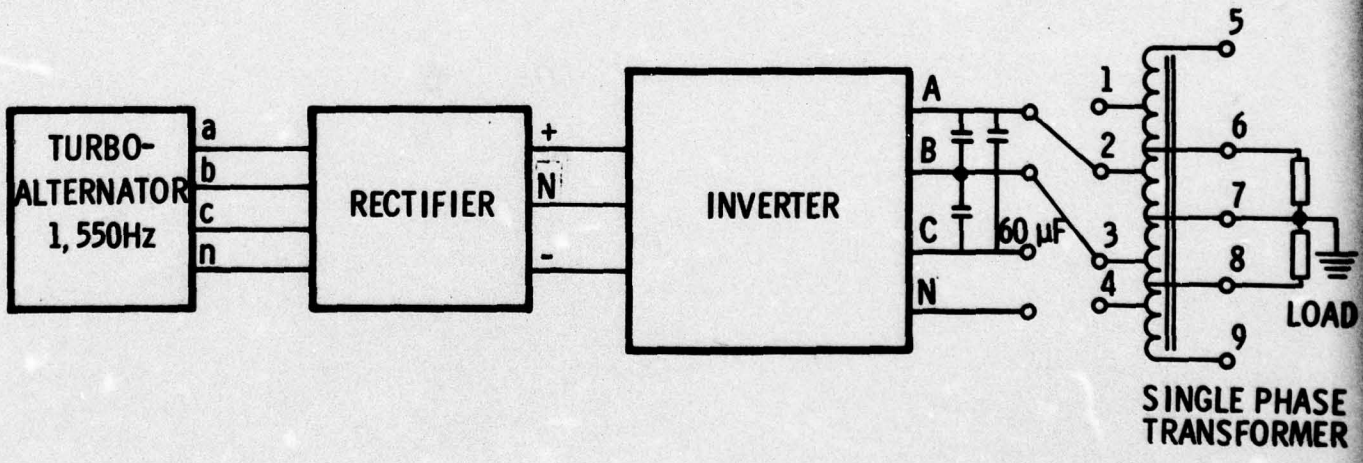


Figure 2-41. Connections for 400 Hz, Single-Phase, Three-Wire Power

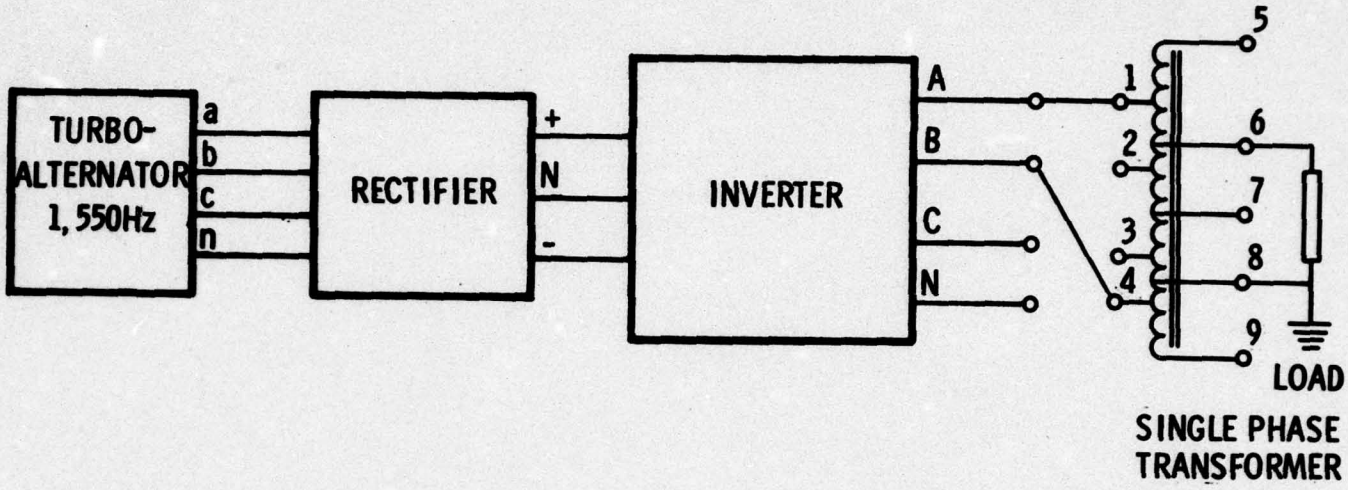


Figure 2-42. Connections for 60 Hz, Single-Phase, Two-Wire Power

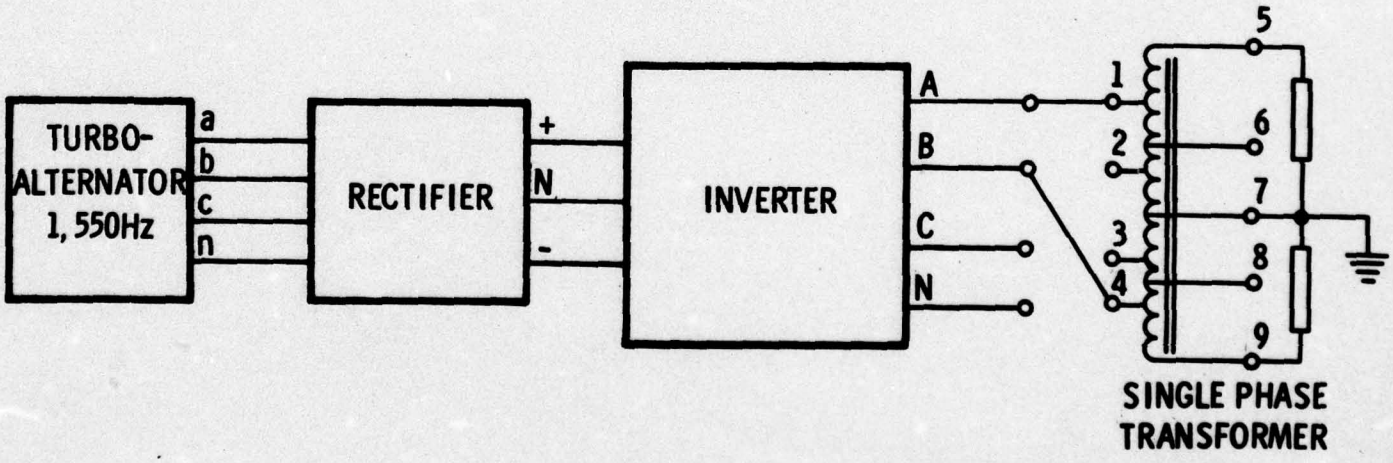


Figure 2-43. Connections for 60 Hz, Single-Phase, Three-Wire Power

Testing of Item No. 0003 and final input and output filter designs were accomplished after Item No. 0004 was completed.

2.3 UPGRADE OF COMMUTATION CAPABILITY (ITEM No. 0004)

The contract work statement required upgrading the commutation capability of the frequency converter (furnished as Item No. 0001) to enhance to the maximum extent possible the operation of the frequency connector when energizing single-phase, 0.5 per unit impedance, low-power factor loads. This effort included, but was not limited to, the step voltage commutation methods developed in Contract DAAK 02-72-C-0338.

The process of forming step voltages in the Delco inverter involves transfer of load current from a conducting thyristor at one voltage level to another at a higher or lower step voltage level. During the commutation interval, load current does not change significantly due to energy stored in inverter inductors or the load.

Methods of step changing in the Delco frequency converter have been based on using a double bus, with each bus connected to alternate steps so that changing of voltage levels resembles ascending or descending a ladder.

2.3.1 ANALYSIS OF Y AND X FUNCTIONS

The Delco frequency converter generates two sets of step voltages which are defined as y and x functions, as illustrated in Figure 2-44a. These functions have a fundamental frequency three times that of the output voltages. The step widths and heights of the y and x functions are derived from sine wave approximations of the frequency changer output voltages. (See Appendixes B and C in Volume II of this report.)

A basic circuit for generating the y and x step voltage functions is shown in Figure 2-44b. When the transformer voltage polarity is positive, the y function switches start at step 4 and generate voltage steps down to the zero level, and the x function switches start at the zero level and generate voltage steps up to step 4. When the transformer polarity is negative, the y function switches start at the zero level and generate negative voltage steps to step 4, and the x function switches start at step 4 and generate negative voltage steps until zero level was reached.

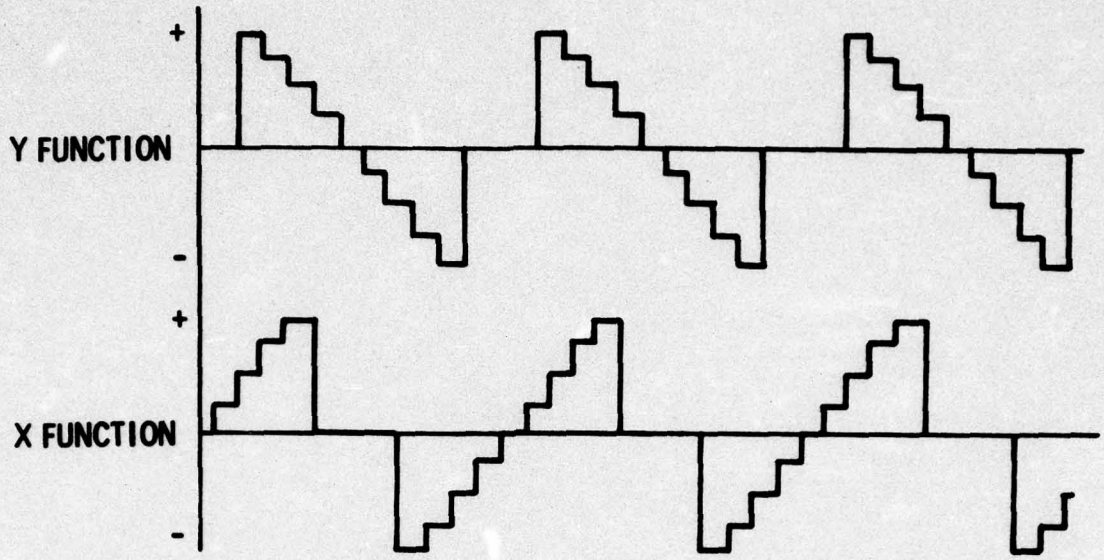


Figure 2-44a. Graphical Definitions of y and x Functions

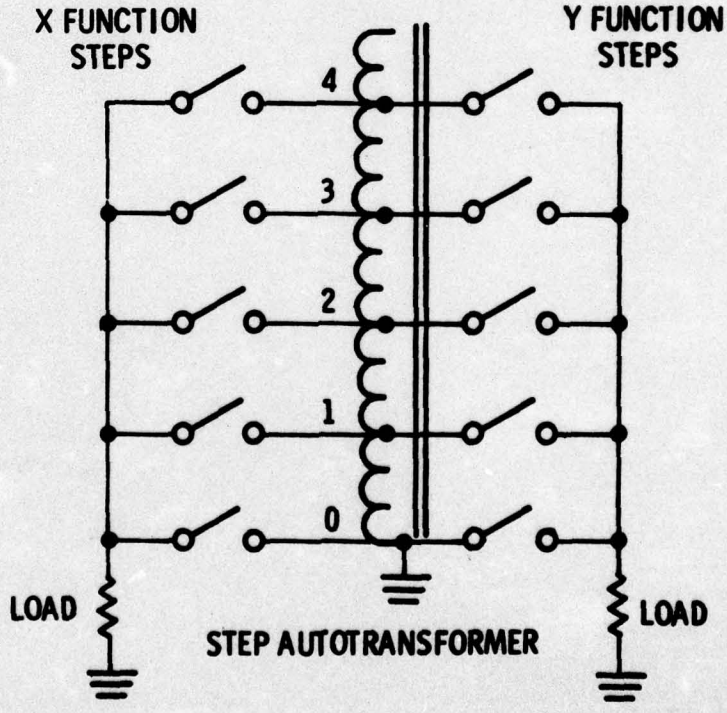


Figure 2-44b. Elementary Step Forming Circuit

Figure 2-45 illustrates a step forming circuit that uses thyristors to shift voltage levels. All combinations of voltage polarities and current flow directions for the y and x functions are illustrated. Analysis of thyristor commutation requirements for conditions 45a and 45h reveals that all required step changes can be achieved with two basic commutation schemes. The following exercise enables one to determine the appropriate commutation scheme for each y and x voltage step change situation. Then it is shown how a complete step forming circuit can be configured.

2.3.1.1 Y Function

In Figure 2-45a, where voltage and current flow positive, it is desired to transfer the current flow from SCR4 to SCR3 in accordance with the y waveform definition of Figure 2-13a. SCR3 is maintained biased off by the conduction of SCR4; therefore, an auxiliary circuit is required to commutate SCR4.

In Figure 2-45b, where voltage is positive and current flow is negative, it is desired to transfer current flow from SCR4 to SCR3. Turning on SCR3 reverse biases SCR4, causing it to turn off, and current flow to transfer to SCR3. Commutation of this type does not require auxiliary turn off circuits and will be referred to as free commutation throughout this analysis.

Voltage and current flow are negative in Figure 2-45c, and it is desired to transfer current flow from SCR3 to SCR4. Turning on SCR4 reverse biases SCR3, and there is free commutation. In Figure 2-45d, voltage is negative and current flow is positive. An auxiliary commutation circuit is required to transfer current flow from SCR3 to SCR4.

3.2.1.2 X Function

In Figure 2-45e, voltage and current flow are positive and it is desired to transfer current flow from SCR3 to SCR4 in accordance with the x waveform definition of Figure 13a. Turning on SCR4 reverse biases SCR3 and there is free commutation.

Voltage is positive and current flow negative in Figure 2-45f, and an auxiliary commutation circuit is required to transfer current flow from SCR3 to SCR4.

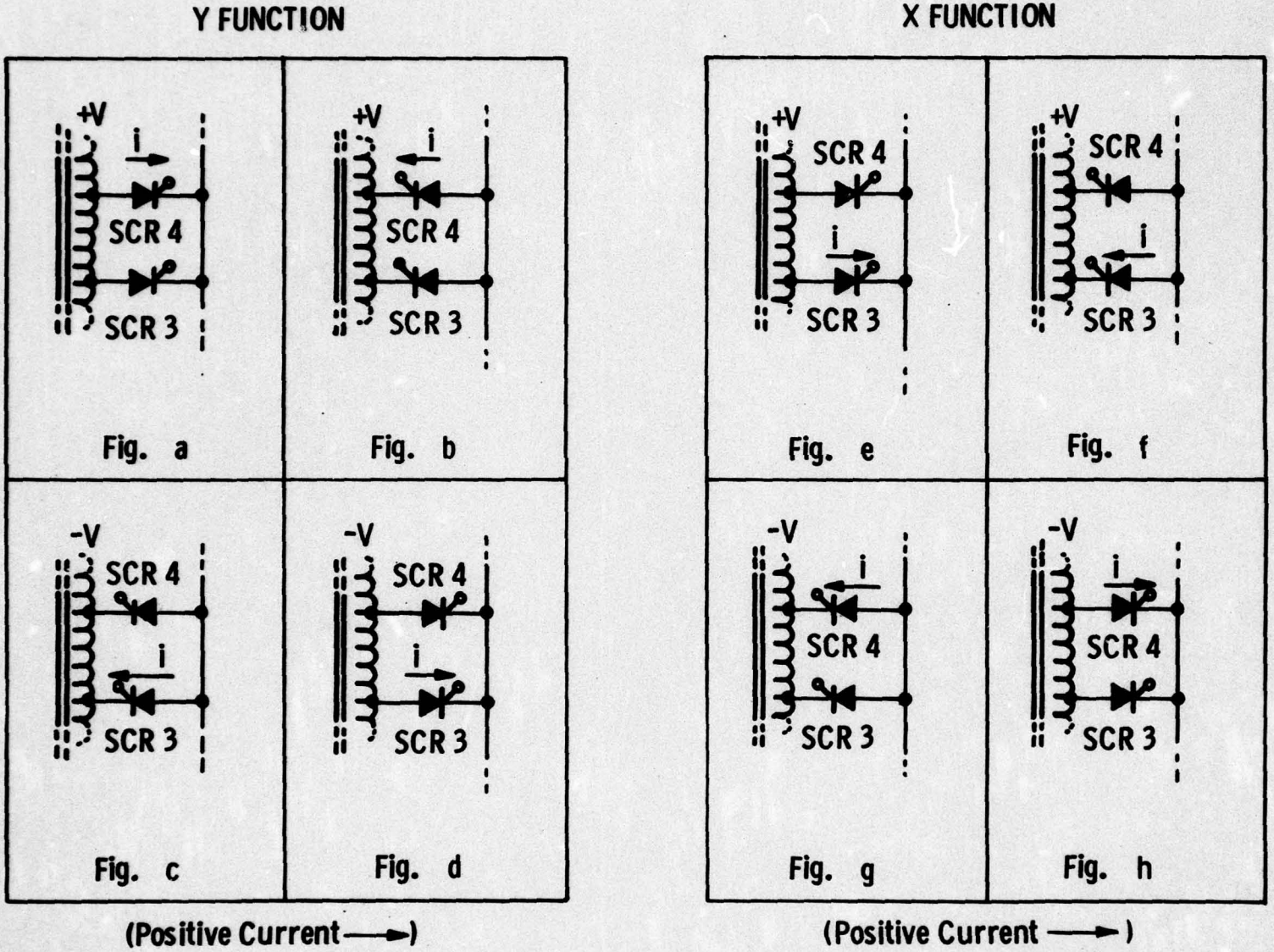


Figure 2-45. Basic Thyristor Step Forming Circuit

In Figure 2-45g, voltage and current flow are negative and an auxiliary commutation circuit is required to transfer current from SCR4 to SCR3.

In Figure 2-45h, voltage is negative and current flow is positive; turning on SCR3 reverse biases SCR4, and there is free commutation.

Tables 2-3 and 2-4 summarize the two methods of commutation for all steps formed by the y and x voltage functions. This information made it possible to configure an improved step forming circuit for the 10 kW frequency converter, as shown in Figure 2-46b, compared to the original circuit of Figure 2-46a. The new circuit improves efficiency two ways:

- By eliminating a diode in series with the step current flow
- By utilizing free commutation.

The free commutation bus creates a path that allows load current to bypass the commutation transistors one half the time and, consequently, reduces transistor heating.

Another benefit is the capability to phase shift the step current to reduce peak transistor current. This phase shift is accomplished by adding capacitance to the output of the inverter. The advantages of doing this are twofold: higher inverter power rating for a given transistor current rating, and improved quality of the output voltage waveform. The penalty for reducing transistor peak current, however, is reduced inverter efficiency because the percentage of power handled by the "center" thyristors is reduced.

Figure 2-47 shows the shift of inverter current with respect to voltage as the output capacitance is increased. Inverter efficiency is maximum when the inverter voltage and current are in phase, as shown in Figure 2-47a. For this condition, more than 80% of the power goes through the "center" thyristors. Shifting the current, as shown in Figures 2-47b and 47c, causes more of the load power to be handled by the step forming circuits which have significantly more losses than the "center" circuits. Load current can be forced to flow only through step paths that utilize free commutation, as illustrated in Figure 2-47c. For this condition, transistor current is reduced to zero and the auxiliary commutation step current paths can be eliminated.

y Function	Step Voltage and Current	
Step Transformer Voltage Polarity	In-Phase	Out-of-Phase
+	Aux. Commutation Required	Free Commutation
-	Free Commutation	Aux. Commutation Required

Table 2-3. Methods of Commutation for Steps Formed by the y Function

x Function	Step Voltage and Current	
Step Transformer Voltage Polarity	In-Phase	Out-of-Phase
+	Free Commutation	Aux. Commutation Required
-	Aux. Commutation Required	Free Commutation

Table 2-4. Methods of Commutation for Steps Formed by the x Function

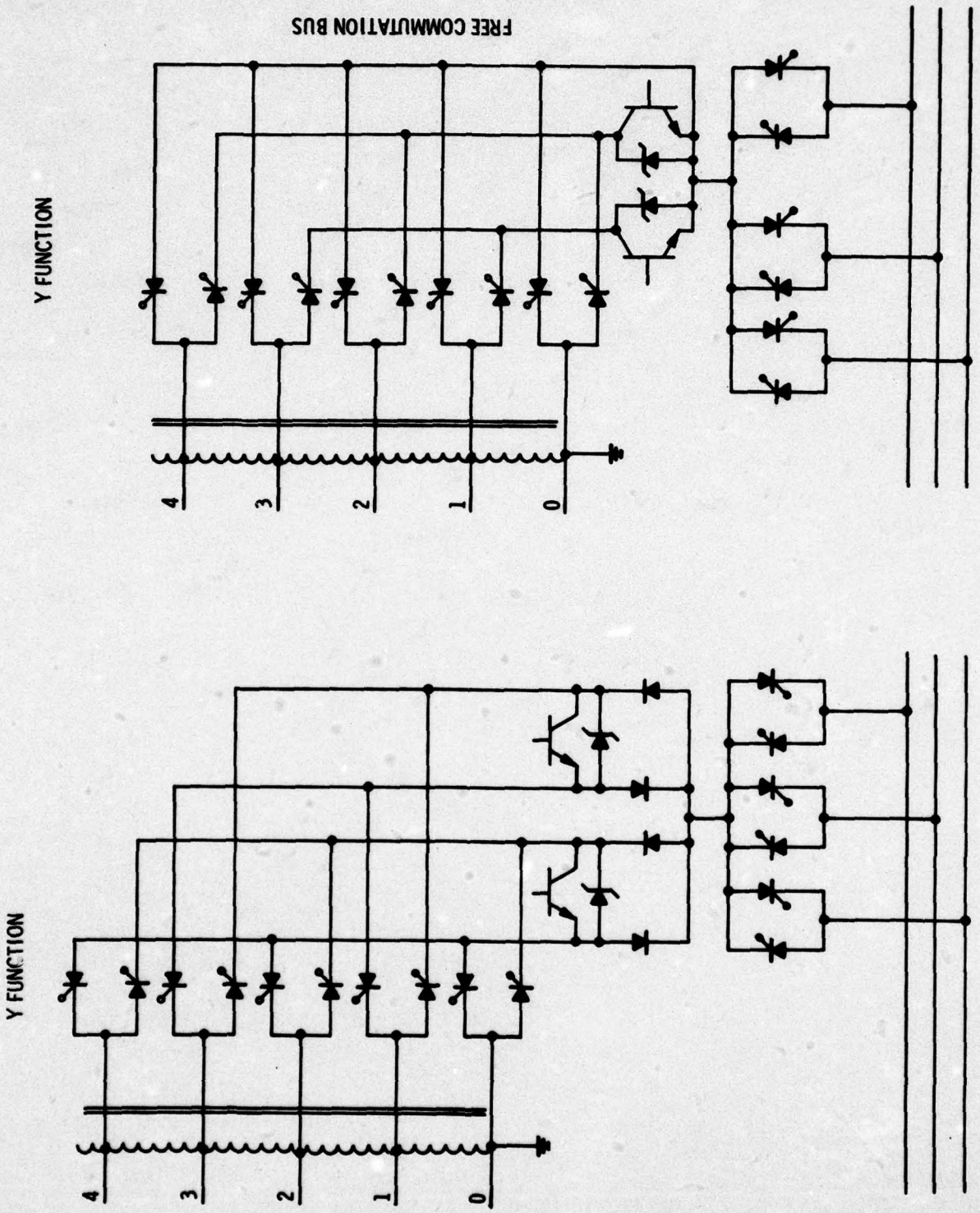


Figure 2-46. Step Forming Circuits

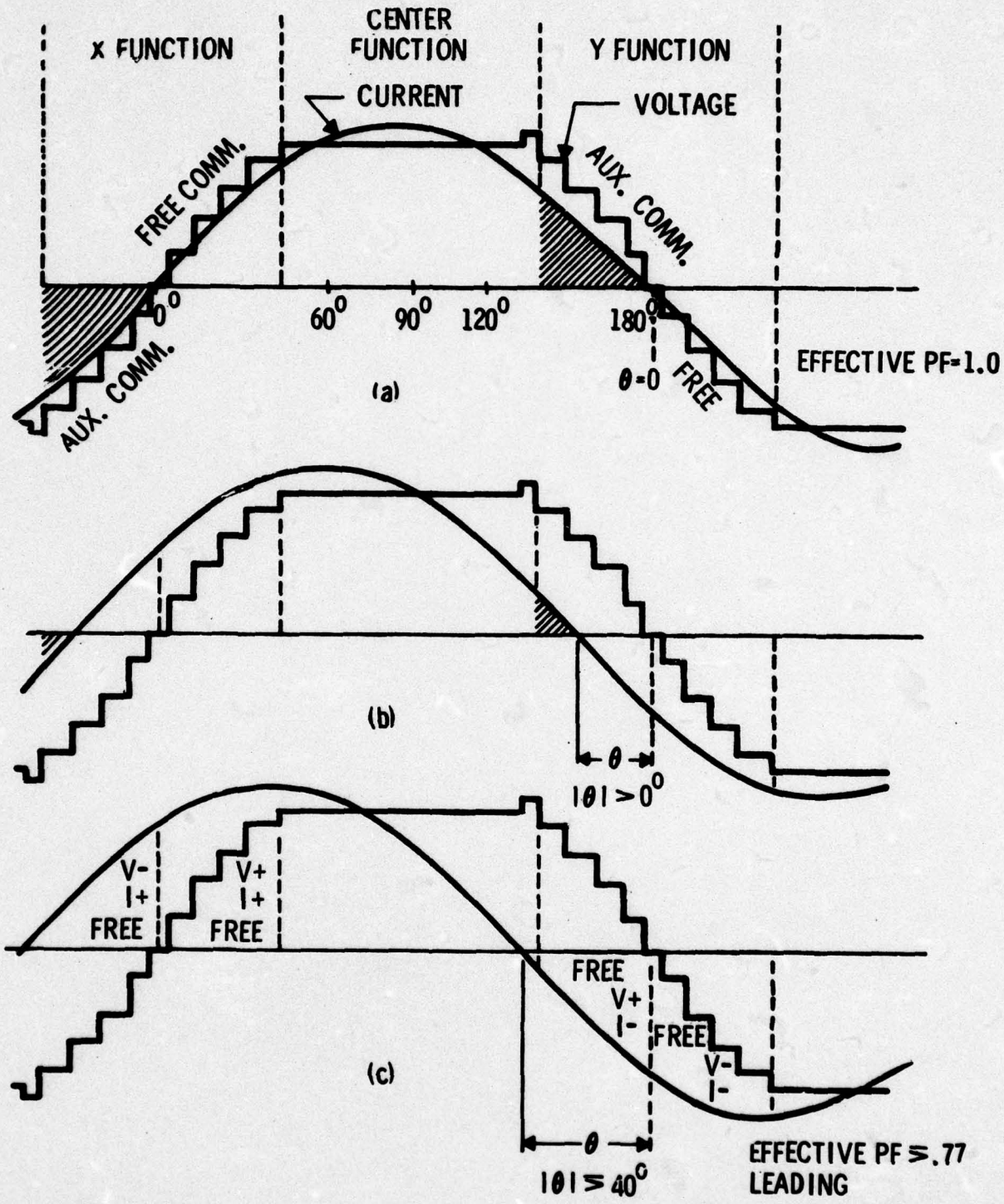


Figure 2-47. Shift of Inverter Current with Respect to Voltage as Output Capacitance is Increased

A schematic diagram of the inverter, as modified by the developments of Item No. 0004, is shown in Figure 2-48. Inverter unfiltered and filtered voltages are shown in the photographs of Figures 2-49 to 2-51. Inverter input and output connections for the three phase tests are shown in the schematic diagrams of Figures 2-52 and 2-53.

2.3.2 INSTALLATION OF THE SYSTEM

Item No. 0001, as modified by Item No. 0004, requires two additional power supplies for breadboard testing:

- A 24 Vdc, one ampere power supply for the T^+, T^- commutation circuit,
- A ± 35 Vdc, five-ampere power supply for the "center" commutation circuit.

The drawing titled "MERDC Power Schematic" shows the commutation power supply connections.

2.4 DISCUSSION OF TEST RESULTS (ITEMS 0003 and 0004)

Detailed test results for Items No. 0003 and No. 0004 are compiled in Volume II, pages 15-85 of this report. Discussed below is the converter's performance with respect to the requirements set forth in the Attachment 3 of the Contract.

2.4.1 CLASSIFICATION (1.2)

The frequency converter produces 10 kW, 0.8 power factor at 400 Hz or 60 Hz for all three-phase or single-phase power connections except 60 Hz, single-phase. For 60 Hz, single-phase the maximum power output is 10 kW at unity power factor and 8.5 kW at 0.8 power factor. The power limitation for this load condition is caused primarily by insufficient energy storage in the inverter input filter. Also, maximum current capability of the commutation transistors is being approached.

2.4.2 VOLTAGE OPERATING RANGE (3.24.1.1)

The frequency converter can produce any output voltage between 95 and 105 percent of rated voltage from no load to full load, at any power factor from unity to 0.8 lagging, except for the load condition noted above.

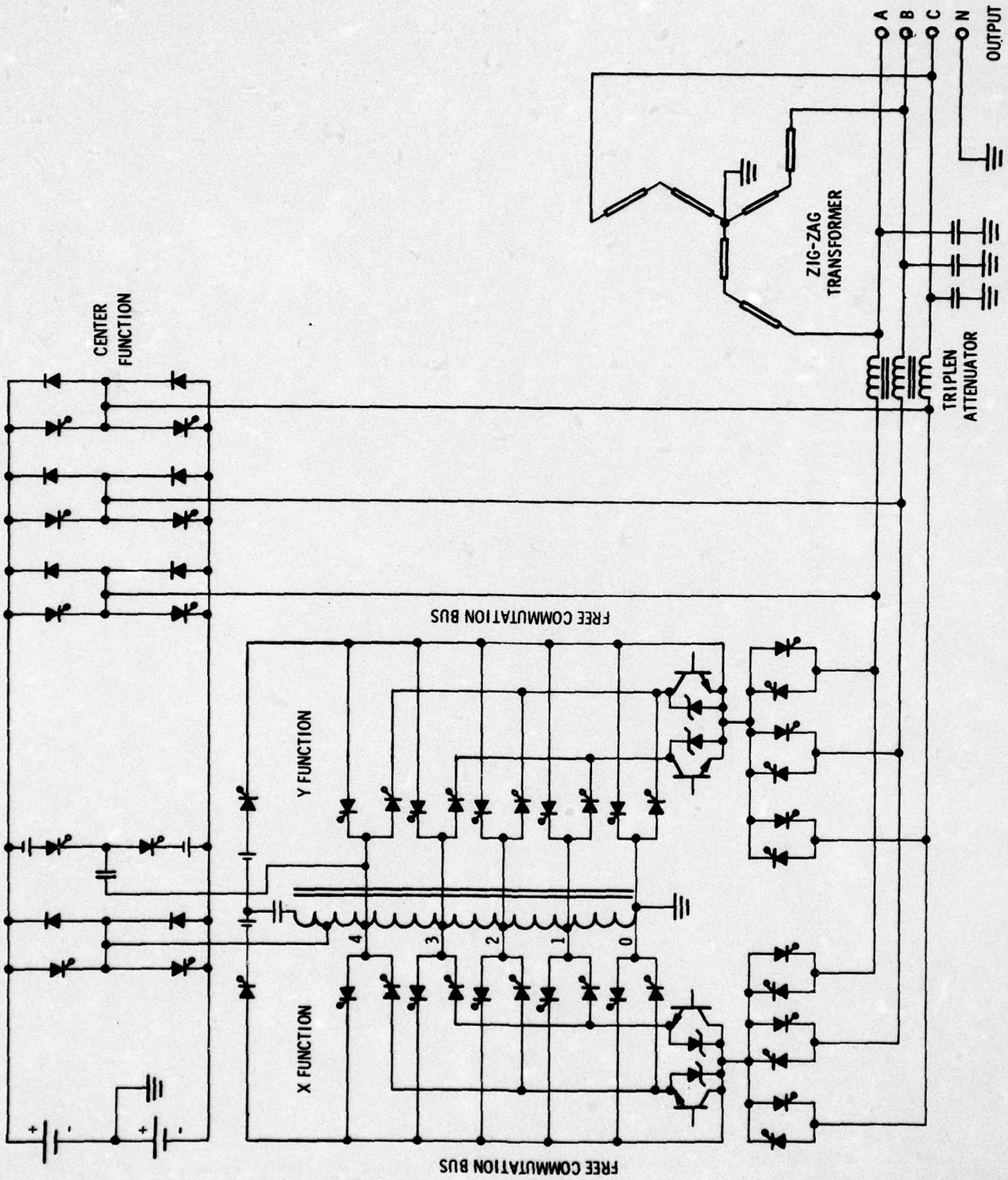


Figure 2-48. MERDC 10 kW Breadboard Frequency Converter Based Upon Improvements of Item No. 0004

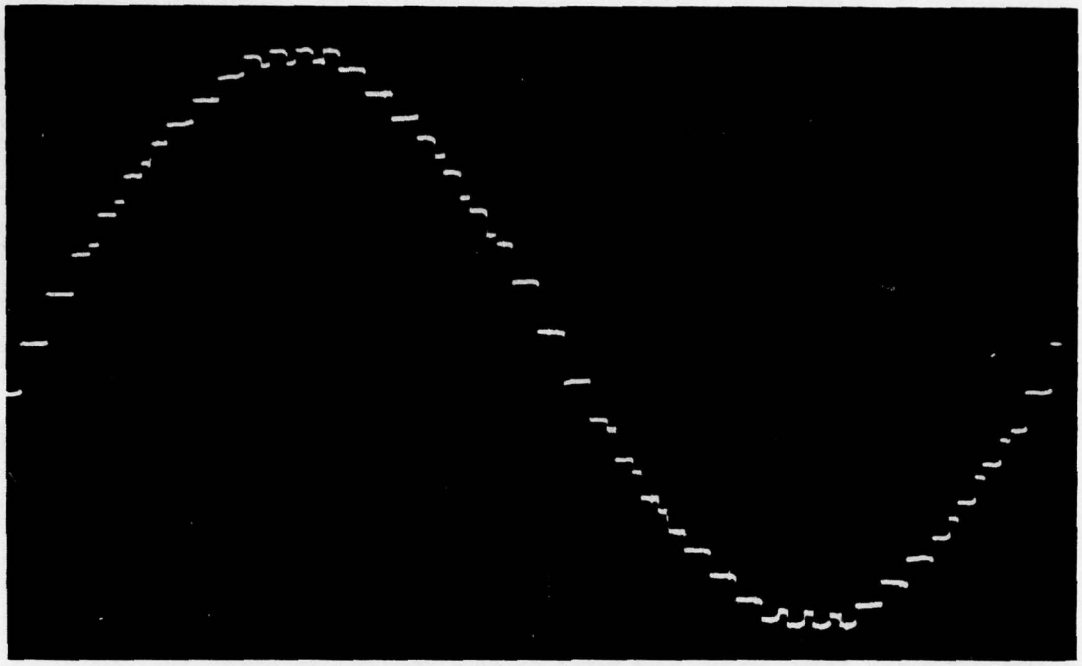


Figure 2-49. Unfiltered Line-to-Neutral Voltage Produced by Inverter as Modified by Item No. 0004

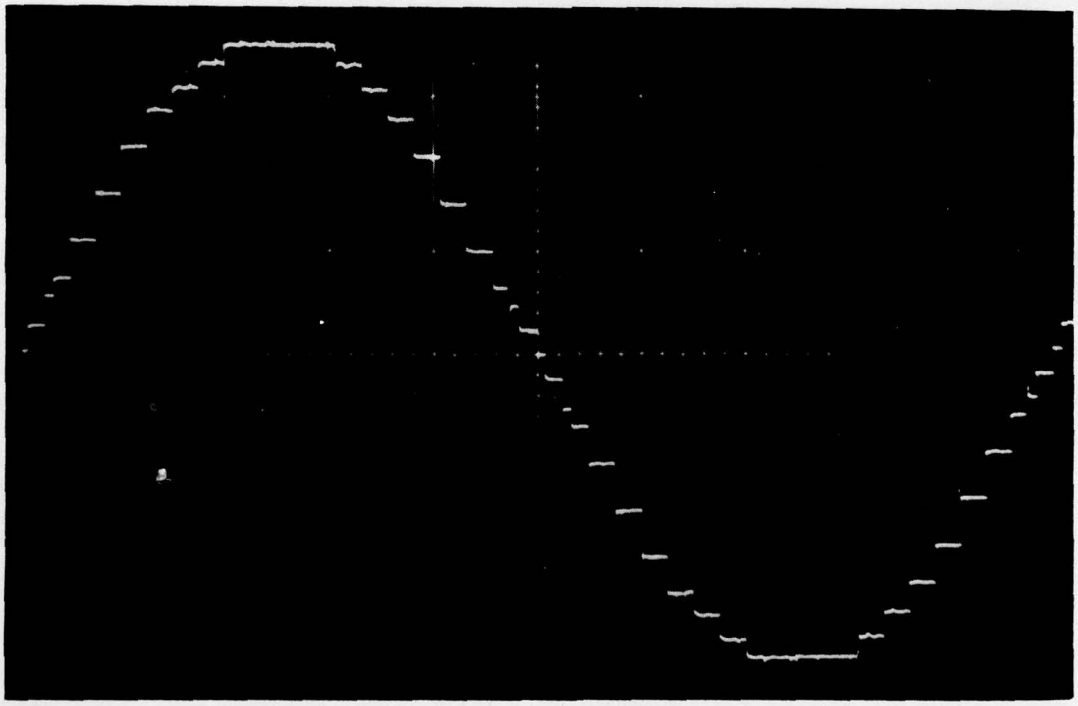


Figure 2-50. Unfiltered Line-to-Line Voltage Produced by Inverter as Modified by Item No. 0004

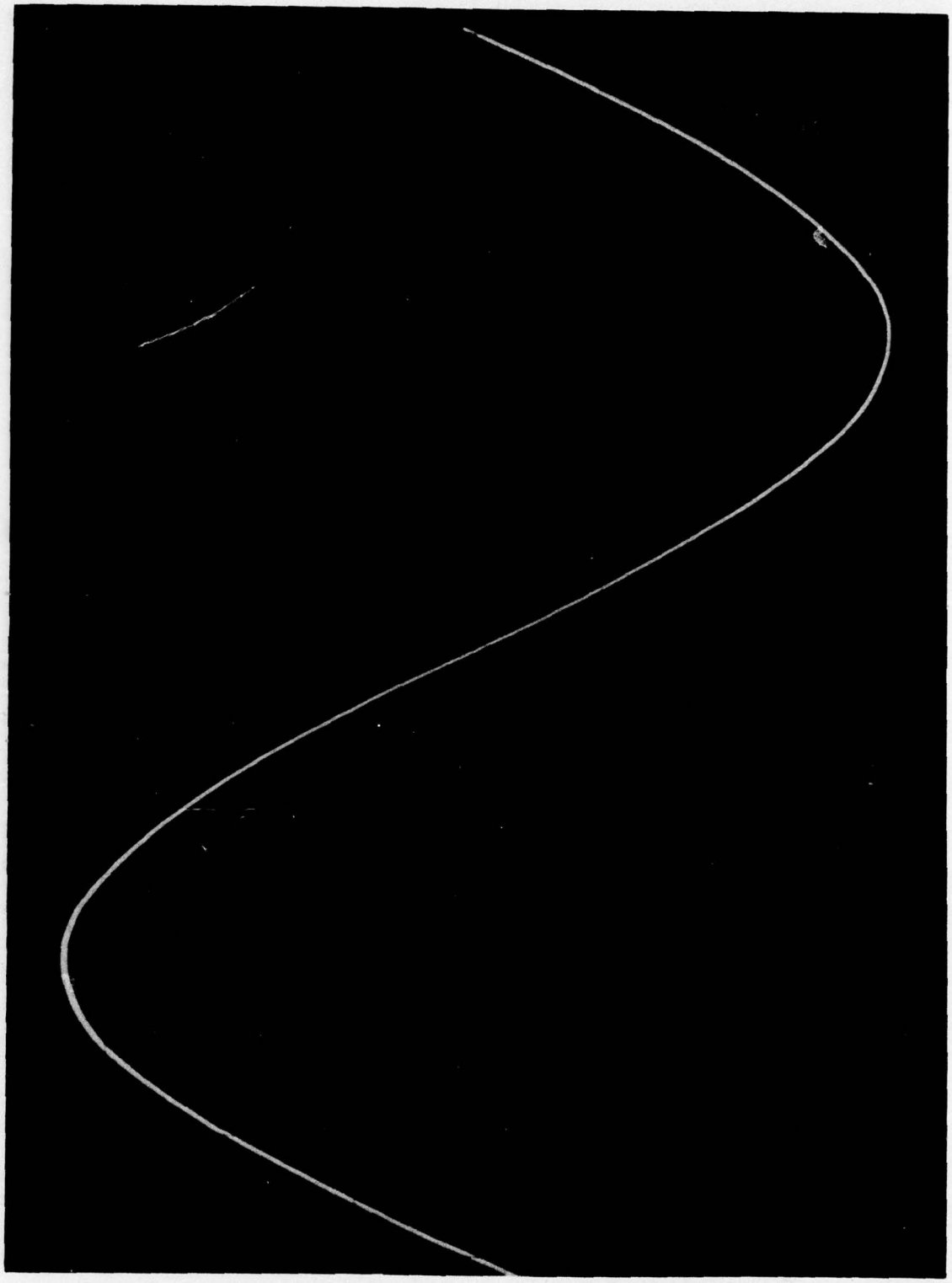


Figure 2-51. Filtered Line-to-Neutral Voltage Produced by Inverter Modified by Item No. 0004
400 Hz, Three-Phase (THD = 0.95%)

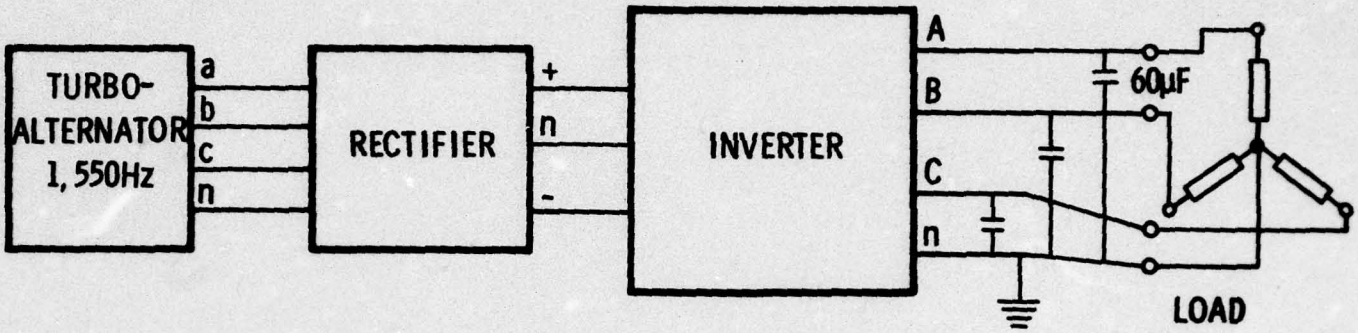


Figure 2-52. Connections for 400 Hz, Three-Phase Power

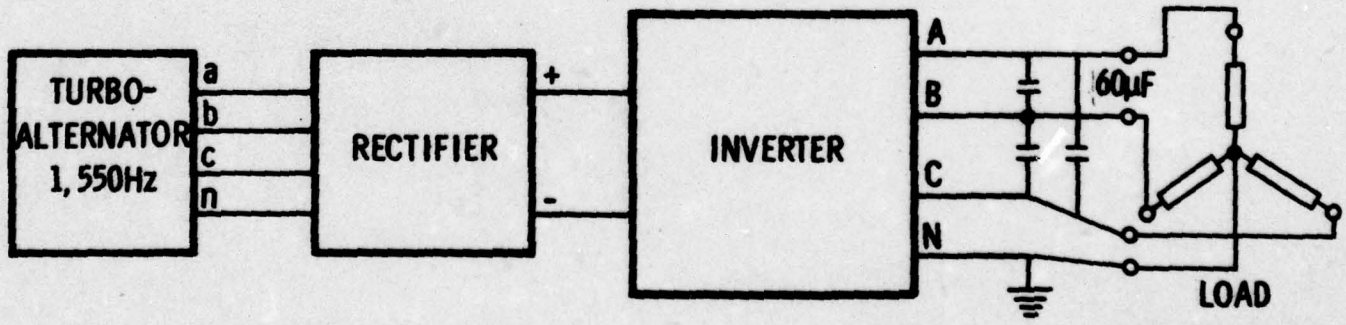


Figure 2-53. Connections for 60 Hz, Three-Phase Power

2.4.3 VOLTAGE WAVEFORM (3.24.1.3)

The deviation factor requirement is met for all modes of operation at 400 Hz. The deviation factor is greater than 5 percent for all modes of operation at 60 Hz. This condition can be corrected by additional development work on the inverter output filter. The harmonics that create the excessive deviation factor are above the 40th. Single harmonics that exceed two percent are as follows:

HARMONICS	PERCENT OF FUNDAMENTAL	FREQUENCY AND NO. PHASES	LOAD kW 0.8 PF
3	4.0	400 Hz, 1 Ø	10
5	2.4	400 Hz, 1 Ø	10
41	2.35	60 Hz, 1 Ø	No Load
3	4.2	60 Hz, 1 Ø	8.5
5	2.2	60 Hz, 1 Ø	8.5
7	2.5	60 Hz, 1 Ø	8.5
41	2.5	60 Hz, 1 Ø	8.5
5	2.38	400 Hz, 1 Ø	No Load
7	2.23	400 Hz, 3 Ø	No Load
41	2.7	60 Hz, 3 Ø	No Load
41	2.5	60 Hz, 3 Ø	11

Improvements in the inverter input filter will reduce the percentage of the third harmonic for single phase, full load operation. Improved output filter designs will reduce all other harmonics that exceed two percent.

The total harmonic content requirement is met for all modes of operation at 400 Hz or 60 Hz, except at 60 Hz, single phase, full load. The input filter characteristics limits performance for 60 Hz, single phase operation. The dc voltage content is less than 100 millivolts for all modes of operation of the frequency converter.

2.4.4 PHASE VOLTAGE BALANCE (3.24.1.4)

The frequency converter meets the phase voltage requirements for all modes of operation.

2.4.5 EFFECT OF UNBALANCED LOAD (3.24.1.5)

The maximum voltage unbalance is 2.45% at 400 Hz and 6.68% at 60 Hz. An improved input filter will reduce the unbalance to below 5%.

2.4.6 PHASE ANGLE BALANCE (3.24.1.6)

The frequency converter meets the phase angle balance requirements for all modes of operation.

2.4.7 VOLTAGE MODULATION (3.24.1.7)

The frequency converter meets the voltage modulation requirement for all operating conditions except 400 Hz, single phase, 10 kW, unity power factor. The maximum voltage difference between adjacent peaks for this condition is about 3.8 volts compared to 3 volts allowable.

2.4.8 VOLTAGE REGULATION (3.24.1.8)

The frequency converter meets the voltage regulation requirements for all modes of operation.

2.4.9 TRANSIENT VOLTAGE PERFORMANCE (3.24.1.12)

2.4.9.1 No Load-to-Two per Unit 0.4 Power Factor Voltage Transient Test

The frequency converter meets the requirement of dropping not less than 60 percent of rated voltage for 400 Hz, single- or three-phase operation. The frequency converter cannot handle two per unit currents for 60 Hz operation because of the current limitations of the step voltage commutation transistors.

2.4.9.2 No Load-to-Rated Load Voltage Transient

The frequency converter meets the requirement of dropping not less than 80 percent rated voltage for 400 Hz single- or three-phase operation. At 60 Hz, the voltage drop is 70 percent of rated voltage for single-phase operation, and 80 percent of rated voltage for three-phase operation.

2.4.9.3 Rated Load-to-No Load Voltage Transient

The frequency converter meets the requirement that the voltage rise not exceed 120 percent of rated voltage for 400 Hz single-phase or three-phase operation. At 60 Hz, the voltage rises to 128 percent of rated voltage for single-phase operation, and 125 percent of rated voltage for three-phase operation. Improving the design of the output filter will enable the frequency converter to meet the 60 Hz voltage transient specifications.

2.4.10 SHORT CIRCUIT (3.24.1.12)

The frequency converter can limit current at 200 percent for three-phase and single-phase line-to-neutral short circuits. However, the specification cannot be met for two-phase line-to-neutral or single phase line-to-line short circuits. The present inverter uses "center" thyristors that have a turnoff time of 15 microseconds. Use of 10 microsecond thyristors would solve the problem.

2.4.11 FREQUENCY

Frequency Requirements (3.24.2) Nominal Frequency Range (3.24.2.1) Frequency Regulation (3.24.2.2) Long Term Frequency Stability (3.24.2.3) Transient Frequency Performance (3.24.2.4) Frequency Modulation (3.24.2.5) Frequency Drift (3.24.2.6)	The frequency converter meets all frequency specifications.

2.4.12 EFFICIENCY (3.24.3)

The Delco frequency converter has peak efficiency when the inverter current is in phase with the inverter voltage. Then, more than 80 percent of the load power goes through the "center " thyristors at 98 percent efficiency. The overall frequency converter efficiency is then greater than 90 percent.

For 60-Hz and 400-Hz, three-phase operation, overall efficiencies greater than 90 percent have been measured. For 60-Hz and 400-Hz, single-phase operation, the overall efficiency of the Frequency Converter is between 80 - 84 percent at full load.

2.5 CONCLUSIONS AND RECOMMENDATIONS FOR ITEMS No. 0001, 0003, AND 0004

The frequency converter breadboard met most of the electrical performance criteria specified in Attachment No. 3 of the contract. Those areas of performance criteria which were not met were close to the requirements. A moderate amount of development effort is required to improve the inverter input and output filter designs. When this effort is accomplished, the frequency converter will meet all voltage and rated power output requirements.

The two per unit current requirement at 60 Hz can be achieved by replacing the step voltage commutation transistors with thyristor reverse bias commutation. The use of faster turnoff "center" thyristors will enable the frequency converter to handle 200 percent short circuit currents for all short circuit connections. The breadboard development effort has advanced to the stage that the basic circuits can be used in prototype turbo-alternator or general purpose frequency converters for Army mobile or base power systems.

2.6 CONVERTER ADAPTATION FOR 3-PHASE INPUT (ITEM No. 0005)

The contract work statement required adapting the frequency converter furnished as Item No. 0001 to operate from 120/208 volts three-phase, 50 or 60 Hz power sources. It was requested that the Frequency Converter meet the electrical performance requirements of Attachment No. 3 of the contract, except that the three phase output rating was changed to 15 kVA. This output performance applied for an input frequency variation of plus or minus 10 Hz, and a voltage variation from plus 10 percent to minus 15 percent in any combination of frequencies and voltages. The attenuation of power perturbations at the input shall be maximixed and the input impedance presented to the line shall be essentially linear.

The effort was accomplished through the following tasks:

- Task 1: Perform an investigation and analysis of practical circuit schemes that can be used to regulate the frequency converter output voltage, attenuate source induced voltage disturbances, linearize input impedance, and provide current limiting.
- Task 2: Develop design data test procedures for the voltage regulator - current limiter system.
- Task 3: Perform design data testing
- Task 4: Analyze test data for inclusion in the final report.

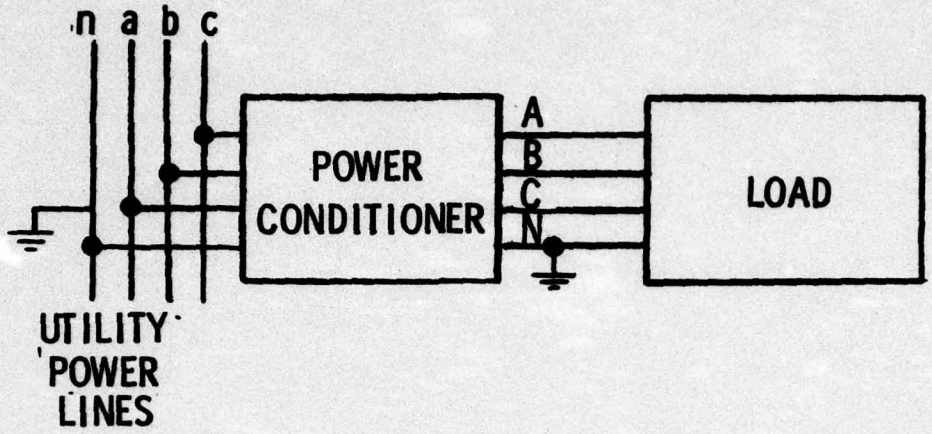
2.6.1 TASK 1: INVESTIGATION AND ANALYSIS

Figure 2-54 is a block diagram showing a power conditioner, input-output connections and load. Also shown are parameters that define the required quality of the input and output power for the power conditioner. The basic Delco inverter produces three-phase or single-phase sine wave voltages at 60 Hz or 400 Hz from dc input power, but does not provide voltage regulation or current limiting.

The present MERDC 10kW breadboard uses a conventional three-phase, full-wave rectifier to provide dc voltages to the inverter. This rectifier generates ac harmonic currents of the order of $6k \pm 1$ (where k is any integer). The purpose of Task 1 is to investigate circuit schemes that reduce rectifier-caused current harmonics to acceptable levels and suitable voltage regulation methods.

The production of current harmonics by three phase rectifier systems is a fundamental problem that has been partially solved for utility and industrial power systems by the use of large filters and multiple-phase rectification techniques. However, these solutions are not always acceptable for military mobile power systems in which excess weight causes performance penalties.

Current harmonics in the utility supply lines are dependent only on the type of rectifier used. Voltage harmonics also depend upon the properties of the utility supply network. The undesirable effects of rectifiers are usually observed in the form of voltage harmonics on the input lines. The following are methods used to reduce current harmonics caused by the rectification of three-phase power.



INPUT SPECIFICATIONS*	OUTPUT SPECIFICATIONS**
40 - 70 Hz utility power 98 - 132 Vrms L-T-N, 176 - 229 Vrms L-T-L, three phase Single voltage harmonics no greater than 2%, or deviation factor greater than 5%, when energized by a 30 kVA, 0.03 P.U. impedance transformer. Performance obtained with input voltage waveforms having a deviation factor up to 10%. Power conditioner efficiency no less than 80%.	120/208 Vrms $\pm$ 1%, three-phase 400 Hz or 60 Hz 15 kVA with 2 P.U. capability -OR- 120 Vrms ± 1%, single phase 120/240 Vrms ± 1%, single phase 400 Hz or 60 Hz 10 kVA with 2 P.U. capability
	Total harmonic content less than 5%. No single harmonic greater than 2%. Able to sustain short circuit currents of 200% for 5 seconds. Output voltages adjustable from 95 to 105% rated voltage.

* USAMERDC purchase description dated July 1969 for "Development of a Family of Electric Power Conditioners"

** Attachment No. 3 of Contract No. DAAK02-72-C-0210

Figure 2-54. Power Conditioner Input/Output Connections and Parameters

2.6.1.1 Passive Filter Methods

Conventional series-resonant filters, as depicted in Figure 2-55, are commonly connected to the ac terminals of the rectifier in order to supply a shunt path for the harmonic currents. Filters tuned to the fifth and seventh harmonics are as shown. The eleventh and higher harmonics are attenuated by line-to-neutral connected capacitors. Independent automatic tuning of each series-resonant filter branch, through variation of the branch inductance or capacitance, can be used to ensure that the filter remains effective for variations in input power frequency (40 - 70 Hz). The ac line filters are, in general, large and not completely effective. Typical line filters for power conditioners achieve reduction of approximately 45% of the fifth harmonic, 85% of the eleventh harmonic, and correspondingly greater reduction in the higher harmonics.

2.6.1.2 Increased Rectifier Phase Methods

By using an input transformer that effectively increases the number of secondary or rectification phases the lower current harmonics can be eliminated. For example, a 12-phase rectification scheme will theoretically not generate 5th or 7th harmonics. The magnitudes of the remaining harmonics will be equivalent to those of a three-phase, full-wave rectifier system. The penalty involved for the rectification of twelve secondary phases is a significant increase in transformer kVA requirements.

2.6.1.3 Multiple Rectifier Load Methods

Current harmonic cancellation can be achieved by phase shifting the input power to several rectifier units. For example, in a system of three equivalent rectified loads, by using phase shifting transformers ahead of the rectifier transformer primaries on two of the three units, a balanced 18-phase system is achieved.

All three units could have delta-connected primaries with the first unit at zero degrees phase shift or reference phase shift, the second with a $+10^{o}$ phase shift transformer. This system can provide effective control of harmonics, but the requirements on the loads and the added transformer weight make this approach suitable primarily for industry.

2.6.1.4 Harmonic Current Injection Methods

The simplest form of rectifier into which triple-frequency current can be injected is the

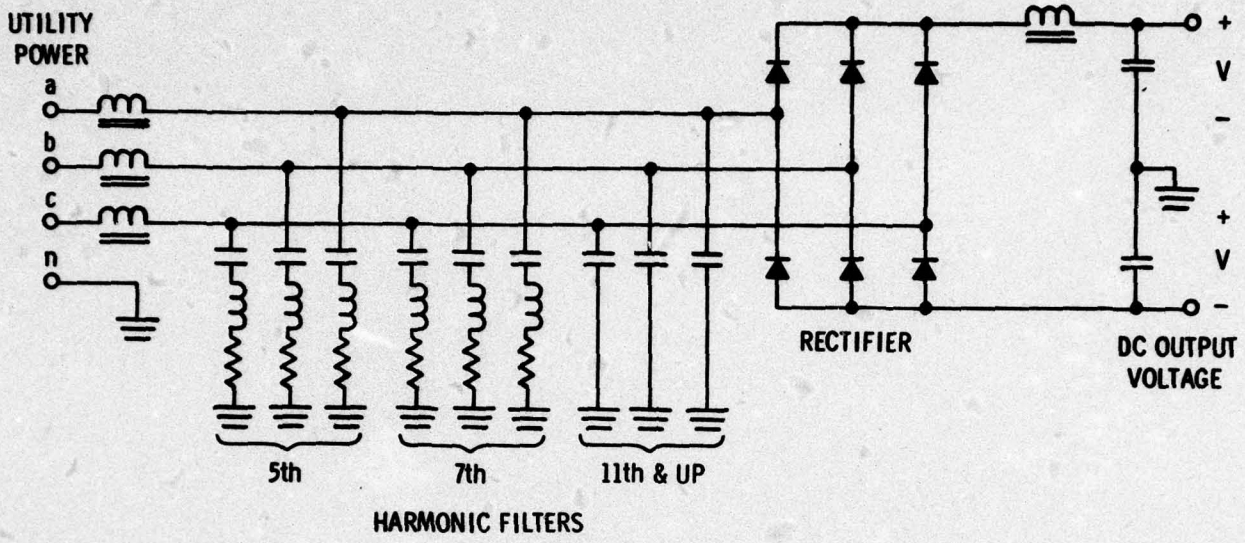


Figure 2-55. Filter Method of Reducing Current Harmonics

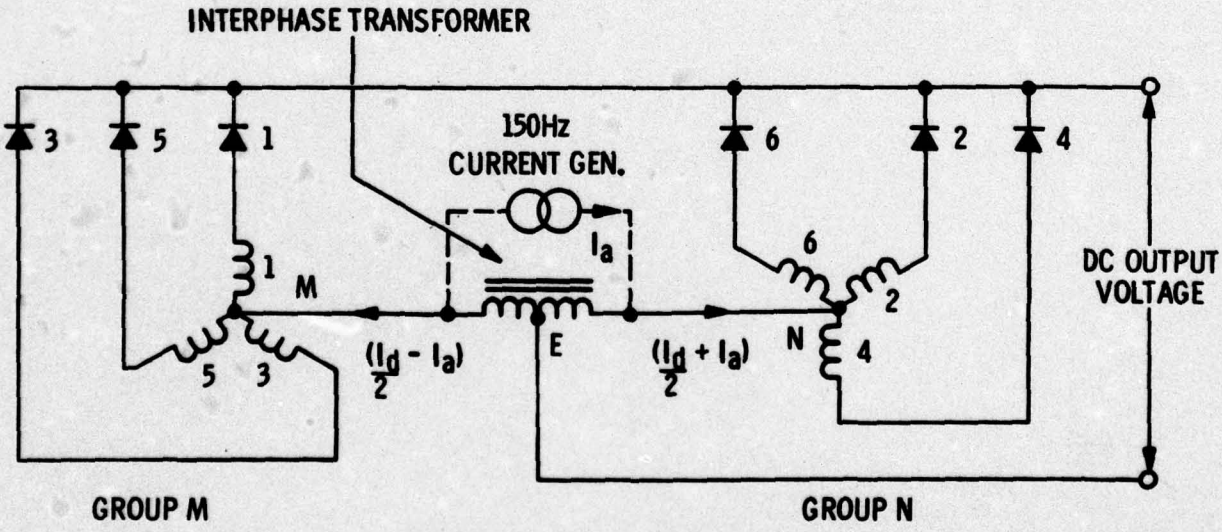


Figure 2-56. Triple-Frequency Current Injection Method, Typical Injected-Current Path at Instant Elements 1 and 2 are Conducting

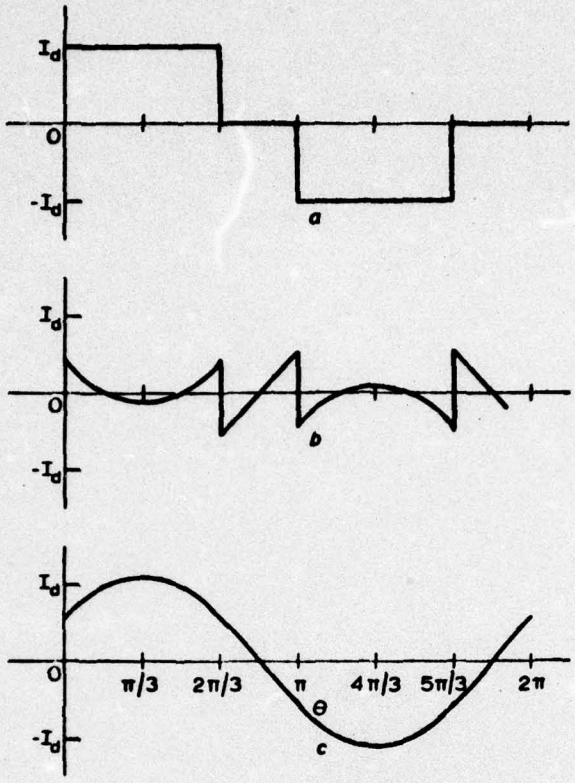
duplex 6-phase circuit shown in Figure 2-56. This circuit is shown with an 150 Hz current generator auxiliary power source that causes triple frequency currents to circulate around the secondary phases of the rectifier, and a corresponding balancing current to flow in the primary of the rectifier transformer.

The amount of harmonic reduction depends on the magnitude of the injected current. The ratio y/h gives a measure of the magnitude of the triple-frequency injection current I_a with respect to the steady load current per group, $I_d/2$. The reduction in harmonics for a variety of injection ratios is shown in Table 2-5. For a y/h ratio of 0.64 the 5th harmonic of the line current is reduced to zero and harmonics from the 7th to 25th are reduced significantly.

Injection ratio y/h	Order of harmonic							
	5	7	11	13	17	19	23	25
0.	20	14·28	9·09	7·69	5·88	5·26	4·35	4
0·64	0	2·8	2·6	2·3	1·83	1·65	1·42	1·3
0·816	5	0	0·84	1	0·83	0·77	0·68	0·63
0·926	7·9	1·7	0	0·18	0·21	0·25	0·28	0·23
0·947	8·5	2	0·19	0	0·1	0·14	0·15	0·15
0·969	9·2	2·4	0·3	0·16	0	0·03	0·06	0·08
0·975	9·3	2·5	0·44	0·2	0·02	0	0·03	0·05
0·983	9·5	2·6	0·5	0·25	0·05	0·01	0	0·03
0·986	9·6	2·7	0·53	0·28	0·07	0·03	0·02	0
0·25	11·7	9·64	6·45	5·44	4·21	3·77	3·13	2·90
0·50	4·12	5·21	3·93	3·42	2·68	2·41	2·01	1·85
0·75	3·25	1	1·57	1·45	1·19	1·1	0·96	0·88
1·00	10·0	2·86	0·65	0·38	0·17	0·12	0·07	0·05

Table 2-5. Harmonics as Percentages of Fundamental with Varying Degrees of Current Injection for Duplex 6-Phase Convertor

A more generalized method of reducing current distortion, than third harmonic current injection, is to inject the required multiple current harmonics into the dc windings of the rectifier transformer. The principle is to modify rectified-current waveforms by an active circuit so that ac line current harmonics are reduced. Figure 2-57 illustrates the principle. Curve (a) is a rectified-current waveform on dc windings and curve (b) is a waveform which consists of every harmonic component of the rectified current shown in curve (a). If the current of curve (b) with an opposite phase is injected in the dc winding, the waveform of curve (c) is obtained, which is the fundamental current.



Principle of generalized method

(a) Rectified current

(b) Current waveform, which consists of all harmonic components of a.

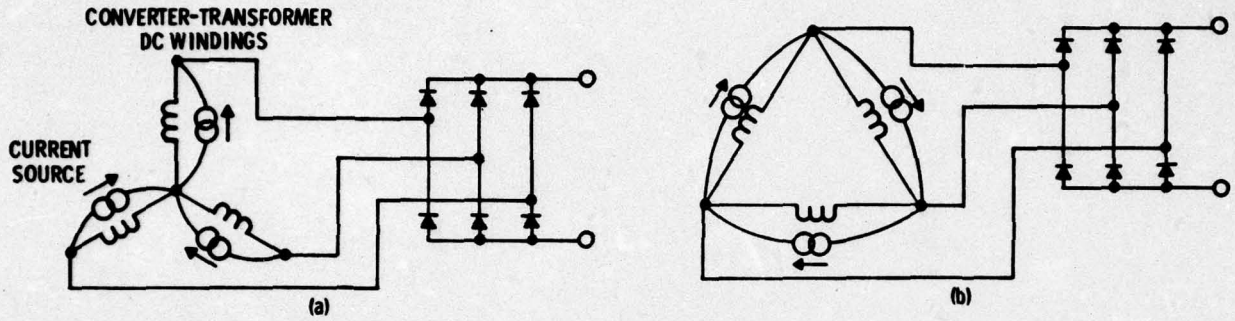
(c) Current waveform composed of a with b subtracted

Figure 2-57. Harmonic Current Reduction Principle

A three-phase current source is required for the basic application, as shown in Figure 2-58. Investigations have shown that the generalized current injection method of harmonic reduction can be used on any type of rectifier. Suitable harmonic orders k of an injected current are 3 (2m-1) where m=1, 2, 3, ... Current harmonics of orders higher than 3 (2m-1) are reduced, but those of lower orders are increased. The optimum current will, in practice, be the third harmonic current.

The optimum phase angle of an injected current is zero, and the injected current divided by the direct load current is about 0.3 to 0.5. If the injected current ratio is fixed, to correspond to a certain harmonic component, that harmonic component can be reduced to zero.

The third harmonic, and generalized methods of current injection to reduce line current harmonic distortion, requires 60 Hz input transformers for the rectifiers and solid state amplifiers or rotating machines as current sources.



(a) Current injection for transformer with wye connected DC windings
(b) Current injection for transformer with delta connected DC windings

Figure 2-58. Current Source Requirements

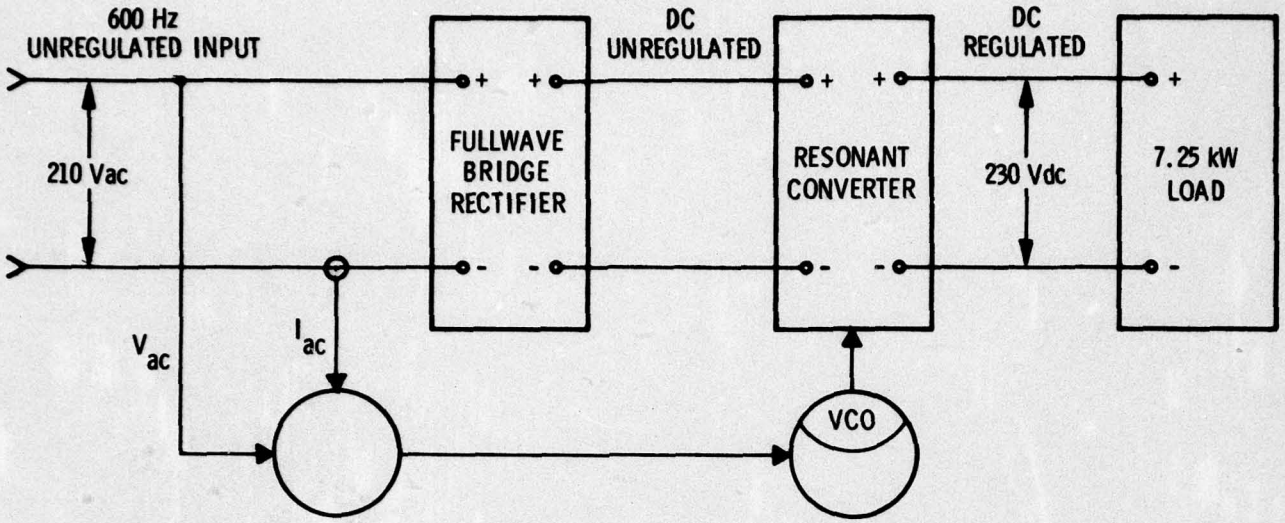
2.6.1.5 Power Switch Methods

Solid state power switch methods make it possible to chop the rectified current and to shape the line current into approximations of a sine wave (fundamental plus high harmonic components). Figure 2-59 is a block diagram of an experimental method of harmonic current neutralization developed by Delco. Utility power is rectified and fed into a resonant converter that shapes the line current as illustrated in the oscilloscope trace..

Power switch systems for reducing current harmonics caused by rectification promise to be light weight compared to the previous systems described. An objective is to combine the harmonic neutralization and voltage control functions into one circuit.

2.6.1.5.1 Voltage Regulation

Delco has developed a small, lightweight, converter which is useful in a large variety of power regulator applications. By virtue of its rapid response and small output filter, this converter functions well in systems requiring voltage source, current source, or both characteristics with good line and load transient recovery. The converter uses twelve SCRs in its power circuit and requires no auxiliary means of commutation.



Block Diagram of Breadboard Circuit

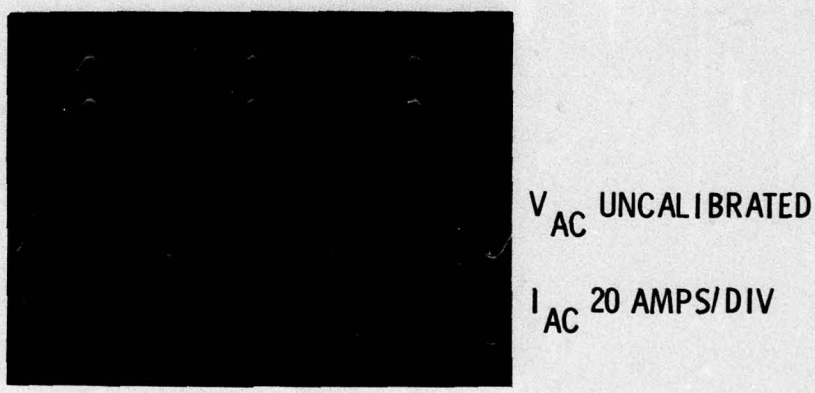


Figure 2-59. Harmonic Current Neutralization

Power output is 15 kW, continuous duty, from a source voltage ranging from 225 V to 375 V. The nominal output voltage is 300 V. The operating efficiency is greater than 92% over a wide range of input voltage and output power. Discussed here, in detail, are the subsystem resonant inverter, development of a four-SCR basic power module, uses of the module, and use in the particular converter.

2.6.1.5.3 A Two-SCR Resonant Inverter

Figure 2-60 shows a simple resonant inverter circuit. L_1, C_1 and R_L constitute a series RLC resonant circuit which is driven by a square wave generated by SCRs Q_1 and Q_2. If Q_1 and Q_2 are triggered at a frequency below resonance, they are commutated. Q_1 generates a positive half-cycle at the end of which the RLC tank circuit current reverses and diode CR_1 conducts. Q_1 is reverse biased and hence, commutated while CR_1 is conducting. Q_2 is triggered some time after Q_1 is reverse biased. The period required for commutation of Q_1 and Q_2 limits the upper operating frequency. For reliable commutation all that is necessary is the assurance that this period is never less than that minimum required by the SCRs chosen for the Q_1 and Q_2 functions. There is no lower limit on operating frequency.

There is a functional relationship between the energy dissipated in the resistor R_L and trigger frequency. This relationship, the only one by which output control is achieved, is smooth and monotonic. R_L may be replaced by an output rectifier, filter, and load as shown in Figure 2-61.

2.6.1.5.4 A Useful Four-SCR Converter Module

The simple circuits of Figures 2-60 and 2-61 are extended to the circuit of Figure 2-62, a full-wave resonant converter. Note that full-wave operation is obtained by triggering Q_1 and Q_4 simultaneously and alternating that triggering with the simultaneous triggering of Q_2 and Q_3. Full-wave operation not only doubles the output power capacity of the converter but also reduces the size of the filter capacitors required. In addition to the extension to a full wave circuit, Figure 2-62 indicates several circuit refinements which have been found to be highly desirable. The primary functions of the additional components are as follows:

- C_s and R_s are RC type snubbers which reduce reapplied dv/dt.
- L_3, L_4, L_5, L_6 aid snubber action, limit di/dt, and reduce turn-on losses.
- T_1 non-dissipatively returns excess commutation energy to the power

supply (or alternately to the load) and augments reverse bias for improved commutation of Q_1, Q_2, Q_3, and Q_4.

- C_3 increases turn-off time.

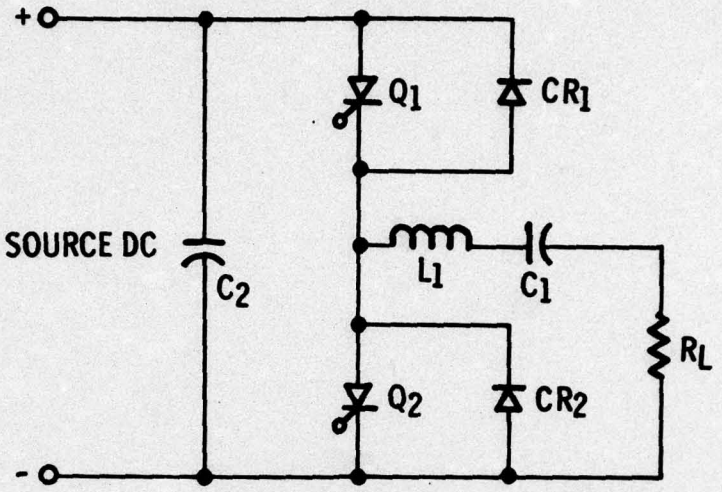


Figure 2-60. A Simple Resonant Inverter

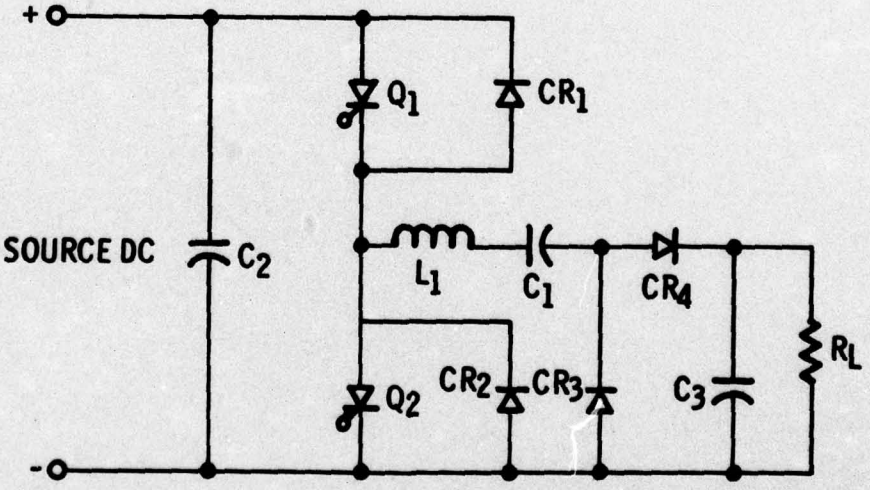


Figure 2-61. A Simple Half-Wave Converter

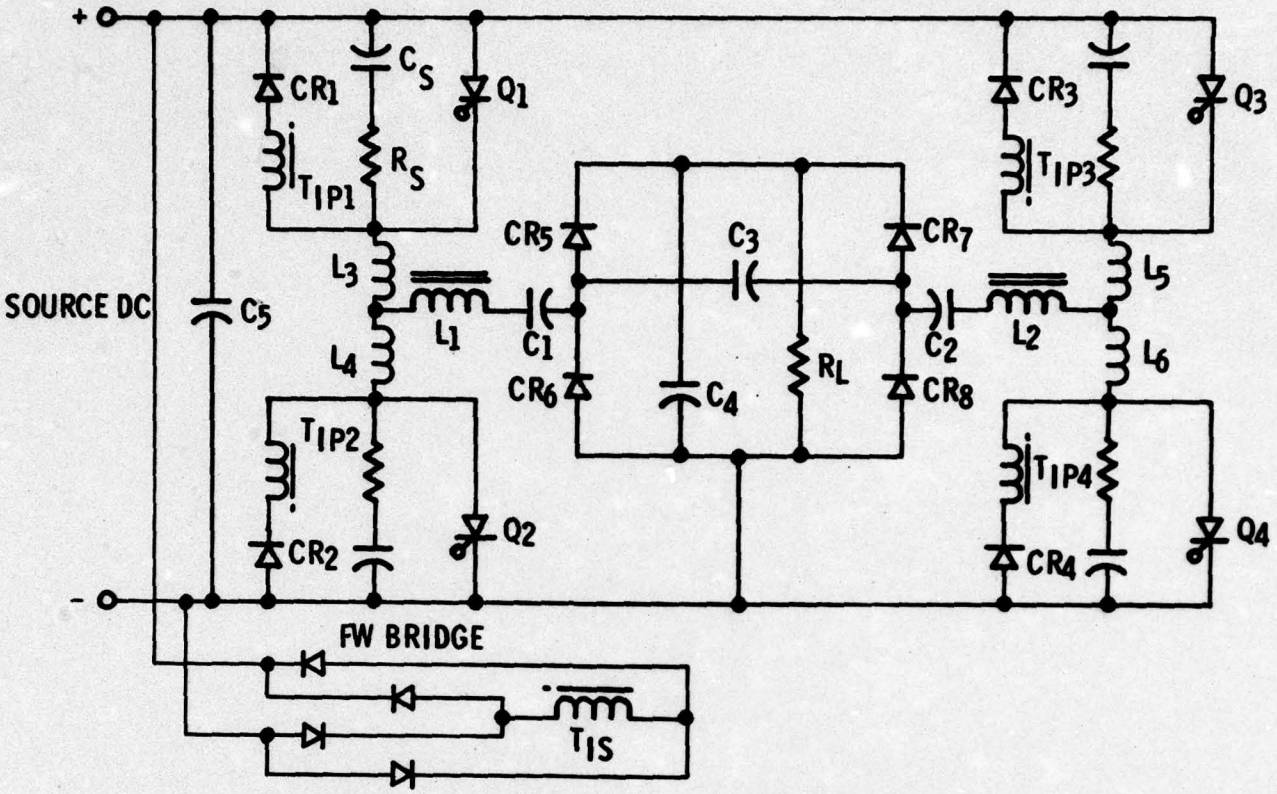


Figure 2-62. A Four SCR Resonant Power Module

The circuit of Figure 2-62 is quite useful for supplying power to well behaved loads; however, rapidly varying loads can cause commutation failure. This problem is circumvented by the use of commutation monitor circuitry which functions as follows:

- The conduction states of Q_1, Q_2, Q_3, and Q_4 are continuously monitored.
- If, for example, Q_1 and Q_4 are conducting, Q_2 and Q_3 are not permitted to receive triggers.
- Q_2 and Q_3 are not permitted to recei ve triggers until Q_1 and Q_4 have been reverse biased at least long enough to assure their ability to block the forward voltage produced when Q_2 and Q_3 are triggered.

2.6.1.5.5 Applications of the Resonant Powe r Module

The four-SCR module has been shown to operate effectively in a wide variety of applications. One application of particul ar interest is in an active, transformerless, harmonic neutralizing approach which was tested in the laboratory. A single phase, 240 V, 60 Hz

source was used as the input to an ac-to-dc-to-dc converter with 300 Vdc output at 10 kW. This module, the heart of the converter, was used for the dual purposes of regulating the output at 300 Vdc and neutralizing the harmonics produced by the rectification process at the input. With a 60 Hz sinewave of input voltage at 1% THD, the input current was observed to be an in-phase sinewave with approximately 3.5% THD. No passive filters were used at the input.

A second application involves the use of an output transformer for step-down, step-up, and/or ac isolation. An eight-to-one stepdown was attempted. A converter supplying from 0 to 35 Vdc at 200 Adc with a 300 Vdc input source was tested. Operation was highly successful and an efficiency in excess of 90% was measured.

2.6.1.5.6 A Twelve-SCR, Six-Pulse Converter

The six-pulse resonant converter now under evaluation uses three of the four SCR modules described above. It is designed to supply well regulated output from 0 to 325 Vdc. The maximum output power is 20 kW at 300 Vdc. The efficiency is typically between 92% and 95% over a wide range of input voltage and output power. The nominal output ripple frequency is 36 kHz and it goes as high as 55kHz. The converter's response characteristics (now under study) are clearly fast; it goes from zero output voltage to 300 V output with a 15 kW load in less than 200μs.

Figures 2-63, 2-64, and 2-65 are plots of measured data - control characteristics, efficiency, and SCR turn-off time. A block diagram of the control circuitry for the six pulse converter is shown in Figure 2-66. It is implemented with digital and analog integrated circuits digital portions were originally TTL logic, but are being replaced with CMOS logic.

2.6.2 TASK 2: DATA TEST PROCEDURES

The MERDC 15kVA inverter and Delco voltage regulator-current limiter were connected as a power conditioner system, as illustrated in Figure 2-66. For the experimental tests the resonant converter functioned to regulate the frequency converter output voltage and to limit current into the frequency converter for overload conditions. No attempt was made to neutralize utility power line harmonic currents. Tests conducted

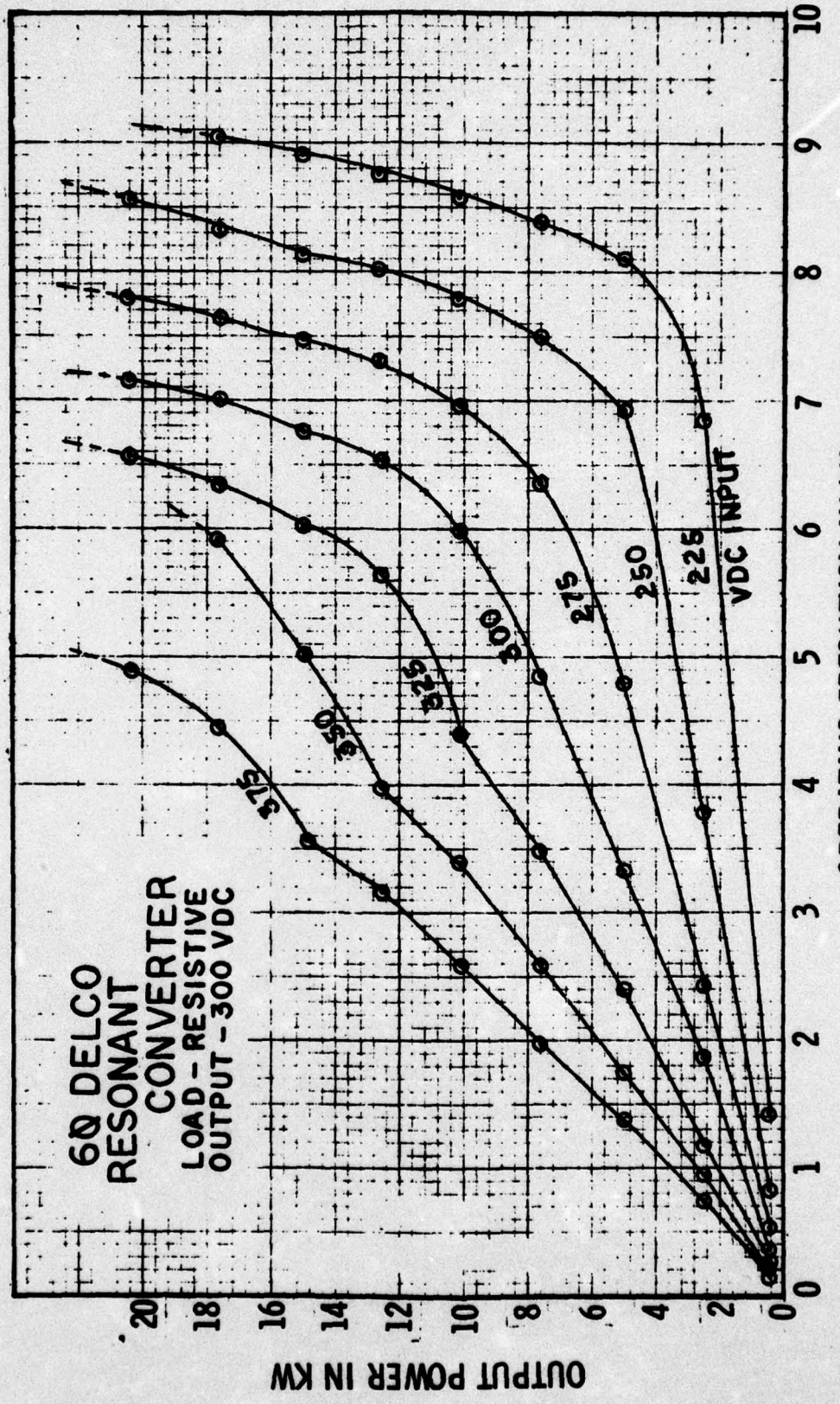


Figure 2-63. Control Characteristics, Frequency Versus Output Power.

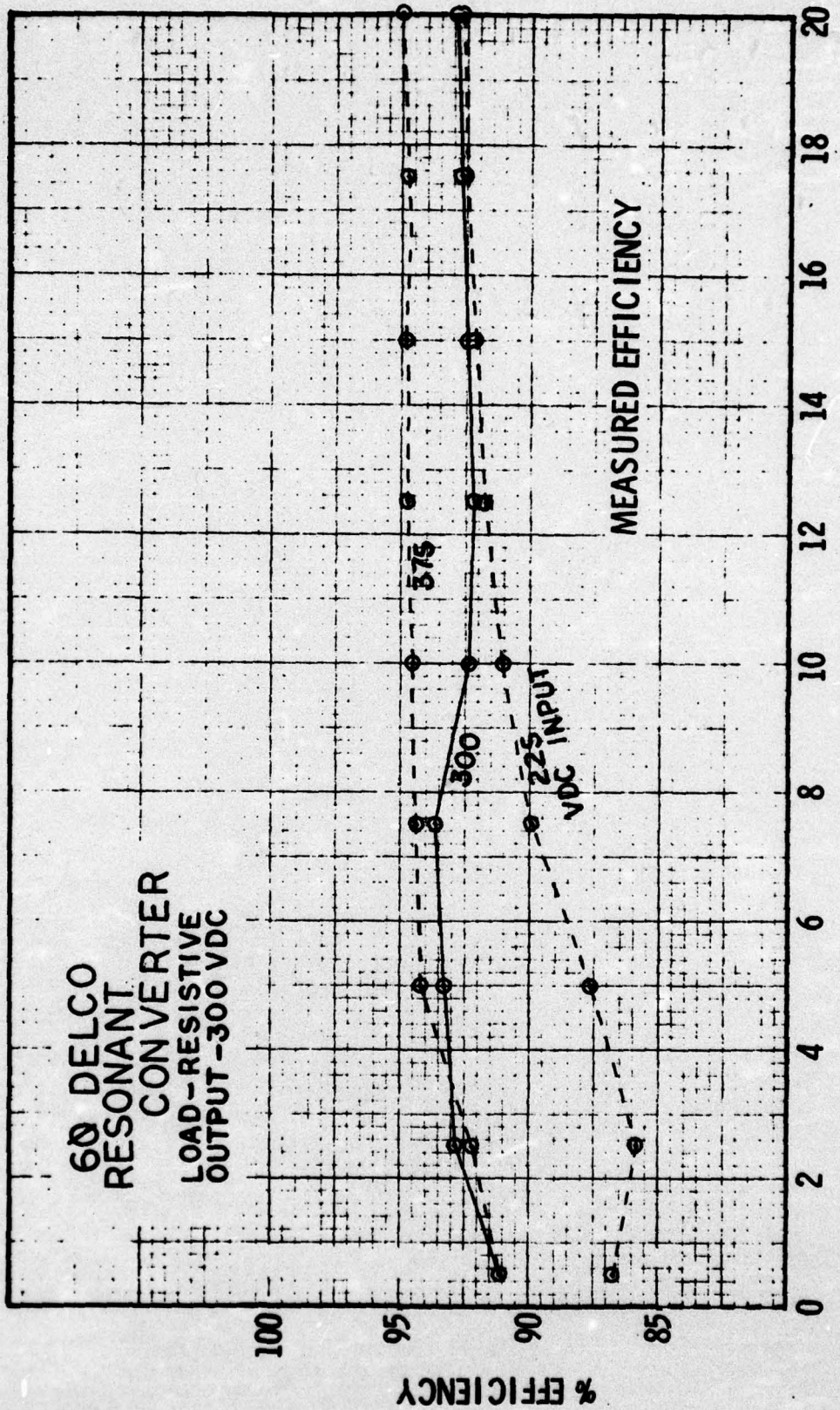


Figure 2-64. Converter Efficiency Versus Output Power.

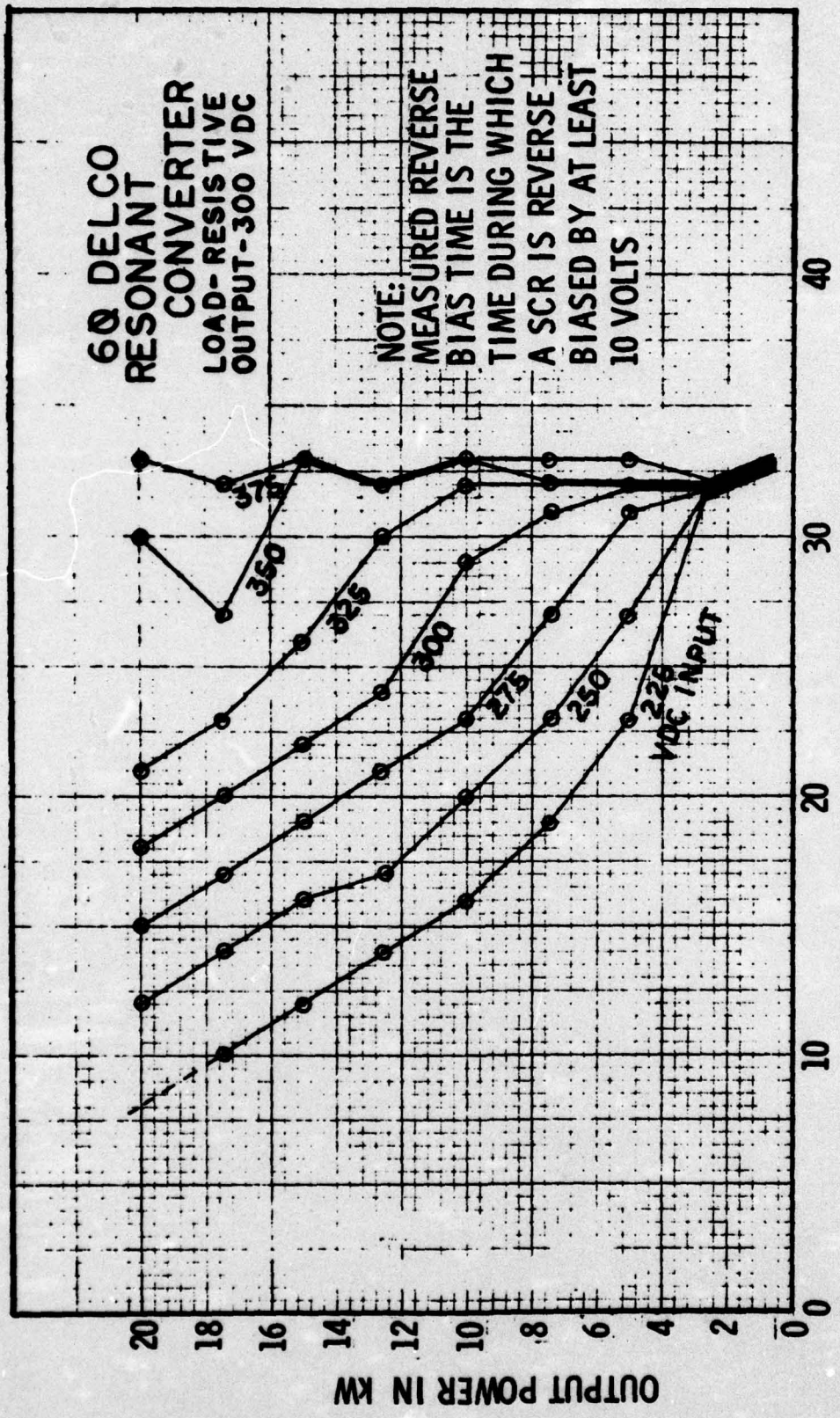


Figure 2-65. SCR Reverse Bias for Various Operations Modes

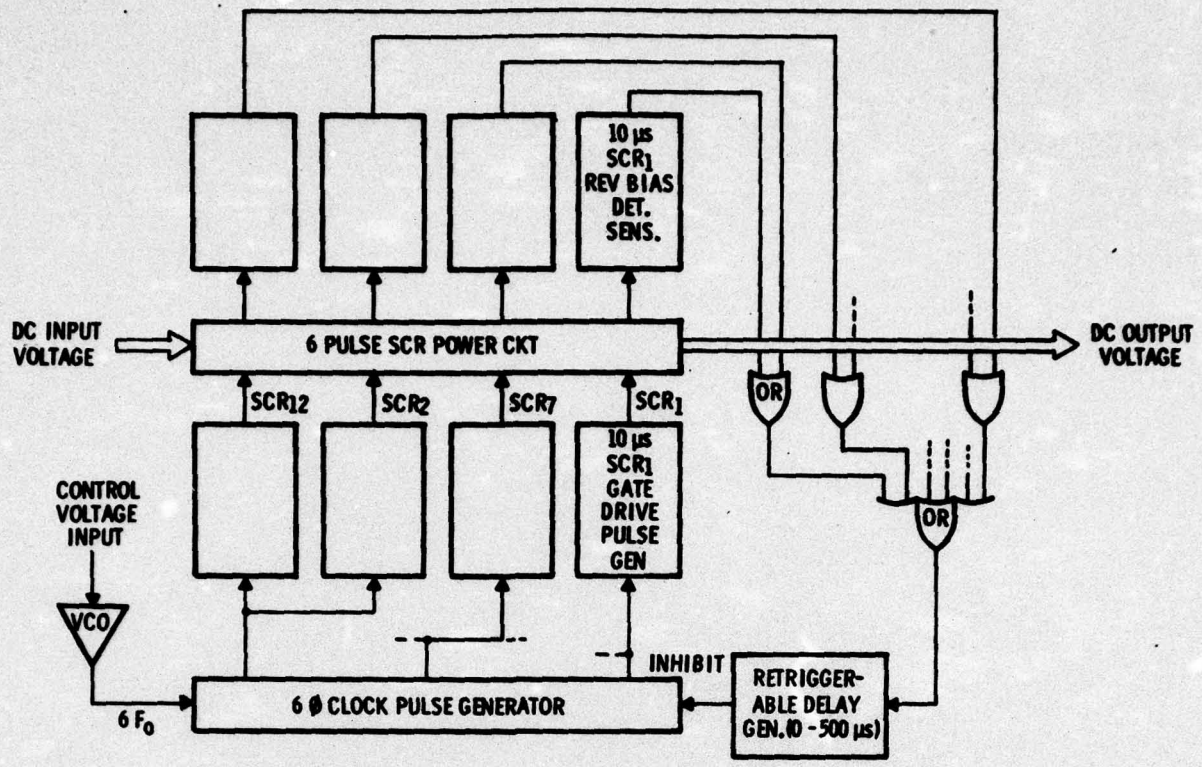


Figure 2-66. Simplified Control for Twelve SCR Converter

were of:

- Voltage regulation for changes in input voltage and load.
- Transient response for abrupt changes in input voltage and load.
- Short circuit current limiting.

These tests were conducted with the frequency converter operating three-phase and single-phase, 400 Hz and 60 Hz.

2.6.3 TASK 3: DESIGN DATA TESTS

All design test data are located in Volume II, pages 125 - 151.

2.6.4 TASK 4: TEST DATA ANALYSIS

The frequency converter produced 15kVA three-phase, or 10kVA single-phase power at 60 Hz or 400 Hz when operated from the laboratory dc power source. (See pages 88 - 121 of Volume II of this report.) Voltage waveform harmonic content, deviation factor and phase balance were essentially as reported in Section 2.4, Discussion of Test Results

(Items 0003 and 0004). This section describes the voltage regulation, source-induced voltage disturbance response, load transient response, current limiting capability and input characteristic test results of the power conditioning system of Figure 2-67.

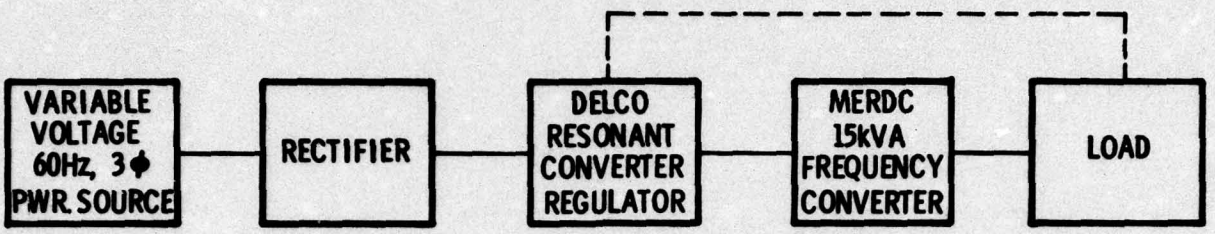


Figure 2-67. Experimental Test Power Conditioner System

2.6.4.1 Three-Phase Operation

2.6.4.1.1 Voltage Regulation

For slow changes in input voltage from plus 10 percent to minus 15 percent of the nominal voltage, and for changes in load from no load to full load, the output voltage of the power conditioner varied less than one half (1/2) of one percent of the 120/208 volts at 60 Hz or at 400 Hz. (See test data and traces of output voltages on pages 126 - 129 of Volume II.)

2.6.4.1.2 Attenuation For Abrupt Changes in Source Voltage

When the source voltage is abruptly changed plus 10 percent or minus 15 percent at 60 Hz or 400 Hz, the output voltages of the power conditioner remain essentially constant. (See oscilloscope traces on pages 130 to 135 and pages 138 to 144 of Volume II.)

2.6.4.1.3 Transient Response for Step Changes in Load

With the power conditioner operating at 60 Hz or 400 Hz and rated voltage, changing the load from no load to 13.2 kW, 0.8 PF caused the output voltage to drop to about 90 percent of rated voltage. (See oscilloscope traces of output voltage on pages 136, 145 and 146 of Volume II.) When the 13.2 kW, 0.8 PF load was suddenly removed, the power conditioner output voltage rise was about 110 percent of rated voltage as illustrated by the photographs. (See oscilloscope traces of output voltage on pages 137, 147 and 148 of Volume II.)

With the power conditioner operating at 60 Hz or 400 Hz, rated voltage and no load the rms terminal voltage dropped to about 80 percent of rated voltage when a 0.4 PF lagging load with an impedance of 0.5 per unit was suddenly applied to the output terminals. (See oscilloscope traces of the output voltage on pages 138 and 149 of Volume II.)

2.6.4.1.4 Current Limiting

Present design limitations prevent the Delco resonant converter from current limiting the output of the frequency converter at 200 percent rated current.

2.6.4.1.5 Power Conditioner Input Characteristics

No attempt was made to neutralize the current harmonics in the utility power lines at the input of the power conditioner rectifier. The three-phase rectifier caused single harmonics of the input voltage waveform to exceed two percent and the deviation factor to exceed five percent. (See oscilloscope traces of utility power line currents and voltages on pages 86 and 87 of Volume II.)

2.6.4.2 Single Phase Operation

The power conditioner output voltage sensing circuit was designed for three-phase operation and could not regulate single-phase voltages adequately. Therefore single-phase voltage regulation and transient tests were not performed. However, single-phase loading of the power conditioner was demonstrated.

The power conditioner energized single-phase loads of 8.8 kW, 0.8 PF (11 kVA) at 60 Hz and 400 Hz. The total harmonic content of the output voltages at full load were 2.65% at 400 Hz and 5.6% at 60 Hz. (See traces of output voltages of the power conditioner for single-phase operation are on pages 150 and 151 of Volume II.)

2.6.4.3 Conclusions and Recommendations for Item No. 0005

The MERDC frequency converter operates effectively as part of a power conditioner system. Some further development is required to reduce deviation factor for 60 Hz operation. Further studies and system analysis are required for power conditioner systems in terms of performing the input current harmonic reduction function and devising low cost circuitry.

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